QUALITY SEMICONDUCTOR, INC.

High Speed CMOS 3.3V 16-Bit Registers (3-State)

QS74FCT163374

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1 μW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5 ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Extended commercial temperature: –40°C to +85°C
- Extended 3.3V supply range 2.7V to 3.6V
- JEDEC compatible LVTTL output levels for 3.3V
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- A and C speed grades: 5.2 ns t_{PD} for C
- 5V tolerant inputs for 5V to 3.3V translation

DESCRIPTION

The FCT163374 is a 16-bit buffered register with three-state output that is ideal for driving address and data buses. The output enable (x$\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers, or one 16-bit register with common clock. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01). Multiple power and ground pins result in low ground and V_{CC} bounce. This JEDEC LVTTL compliant 3.3V device is useful for 5V to 3.3V applications since all inputs will support 5V signals.

Figure 1. Functional Block Diagram

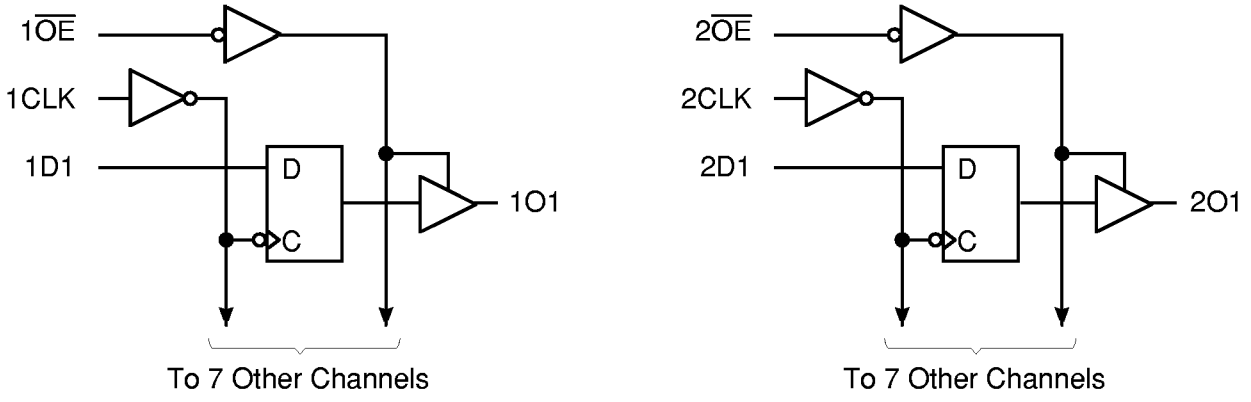


Figure 2. Pin Configuration (All Pins Top View)

SSOP, TSSOP

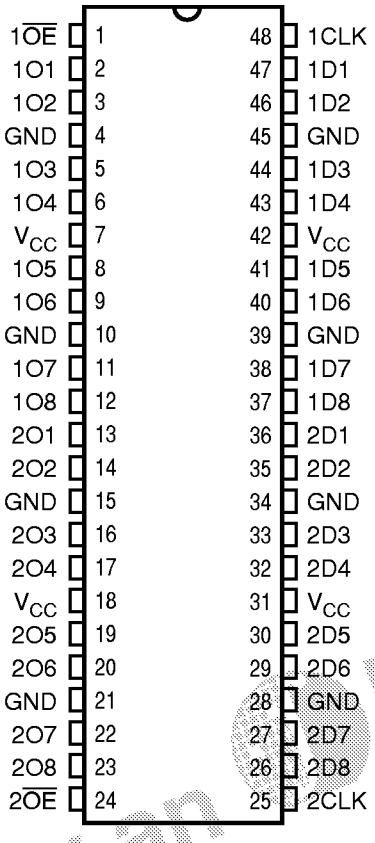


Table 1. Pin Description

Name	I/O	Description
xDx	I	Data Inputs
xOx	O	Data Outputs
xCLK	I	Clock Input
x$\overline{OE}$	I	Output Enable

Table 2. Function Table

Inputs x$\overline{OE}$	Inputs xCLK	Inputs xDx	Internal Q Value	Outputs xOx	Function
H	X	X	X	Hi-Z	Disable Outputs
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	Enable Outputs
H	↑	L	L	Hi-Z	Load Input Data
H	↑	H	H	Hi-Z	Disable Outputs

Table 3. Capacitance

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Symbol	Parameter	Typ	Unit
C_{IN}	Input Capacitance	7.0	pF
C_{OUT}	Output Capacitance	8.0	pF

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to +4.6V
DC Output Voltage V_{OUT} ..... –0.5V to V_{CC} +0.5V
DC Input Voltage V_{IN} ..... –0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns) ..... –3.0V
DC Input Diode Current with V_{IN} < 0 ..... –20 mA
DC Output Diode Current with V_{OUT} < 0 ..... –50 mA
DC Output Current Max. Sink Current/Pin ..... 120 mA
T_{STG} Storage Temperature ..... –65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol		Min	Max	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
V_{IN}	Input Voltage	–0.5	5.5	V
V_{OUT}	Voltage Applied to Output or I/O	0	V_{CC}	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	–40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs		2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs		–0.5	—	0.8	V
ΔV_T	Input Hysteresis[4]	$V_{TLH} - V_{THL}$ for All Inputs		—	150	—	mV
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < 5.5V$		—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{OUT} \le V_{CC}$		—	—	1	µA
I_{OS}	Short Circuit Current[3,4]	V_{CC} = Max., V_{OUT} = GND		–60	–140	–240	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –0.1 mA I_{OH} = –3.0 mA	V_{CC} –0.2 2.4	— —	— —	V
		V_{CC} = 3.0V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –8 mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 0.1 mA I_{OL} = 16 mA I_{OL} = 24 mA	— — —	— — —	0.2 0.4 0.55	V
		V_{CC} = 3.0V $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24 mA	—	—	0.5	V
V_{IK}	Input Clamp Voltage[4]	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V

Notes:
1. For conditions shown as Max or Min use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
3. Not more than one output should be shorted at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not production tested.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[2]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., Freq = 0 V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = V_{CC} –0.6V[3]		2.0	30	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND, f_i = 5 MHz f_{CP} = 10 MHz	V_{IN} = V_{CC}-0.6V V_{IN} = GND	0.5[5]	0.8[5]	mA
		V_{CC} = Max., Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND, f_i = 2.5 MHz f_{CP} = 10 MHz	V_{IN} = V_{CC}-0.6V V_{IN} = GND	2.5[5]	4.0[5]	mA

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input. All Other Inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} = I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = V_{CC} –0.6V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f_{CP} = Clock Frequency.
   N_{CP} = Number of Clock Inputs at f_{CP}.
   f_i = Input Frequency.
   N_i = Number of Inputs at f_i.

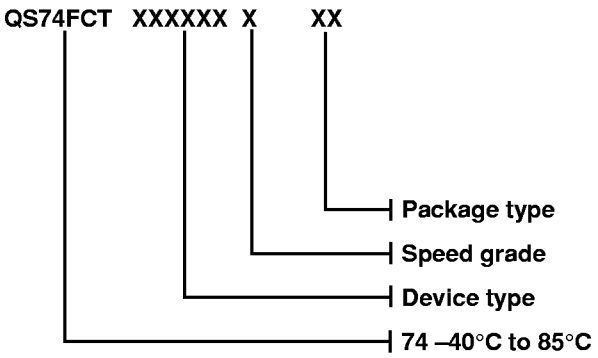
Table 8. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	FCT163374A		FCT163374C		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay xCLK to xOx	2.0	6.5	2.0	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xOx	1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] x$\overline{OE}$ to xOx	1.5	5.5	1.5	5	ns
t_S	Data Setup Time xDx to xCLK	2.0	—	2.0	—	ns
t_H	Data Hold Time xDx to xCLK	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW	5.0	—	5.0	—	ns
$t_{SK(O)}$	Output Skew[3]	—	0.5	—	0.5	ns

Notes:
1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Switching Characteristics are with V_{CC} = 3.3V ±0.3V.
   For 2.7V V_{CC} operation, parameters should be degraded by 20%.
3. Guaranteed by design, but not tested.
4. Skew between any two outputs of the same package switching in the same direction.
   This parameter is guaranteed by design but not production tested.

ORDERING INFORMATION



Device Type:

163374

Speed Grades:

A

C

Package Type:

PV – SSOP,300 mil

PA – TSSOP, 240 mil