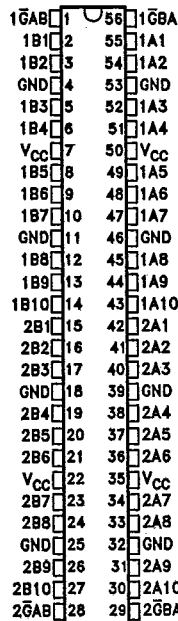


T-52-31
20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

54AC16862, 54ACT16862
 74AC16862, 74ACT16862
 TIO235—D3557, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

54AC16862, 54ACT16862 ... WD PACKAGE
 74AC16862, 74ACT16862 ... DL PACKAGE
 (TOP VIEW)



description

The 'AC16862 and 'ACT16862 are inverting 20-bit bus transceivers composed of two 10-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs (1GAB, 2GAB, 1GBA, and 2GBA). The control logic also allows for isolation and latching.

The 74AC16862 and 74ACT16862 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16862 has CMOS-compatible input thresholds. The 'ACT16862 has TTL-compatible input thresholds.

The 54AC16862 and 54ACT16862 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16862 and 74ACT16862 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OPERATION
GAB	GBA	
L	H	A to B
H	L	B to A
H	H	Isolation
L	L	Latch A and B (A = B)

PRODUCT PREVIEW

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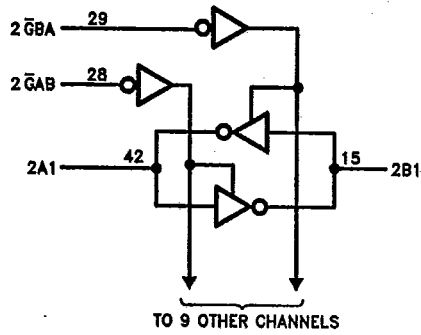
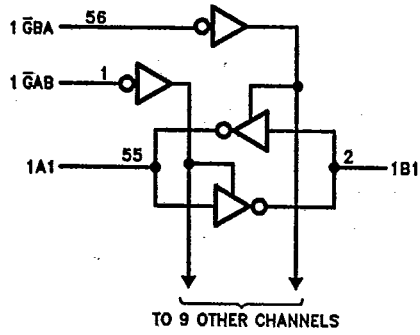
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 DS557, JUNE 1990—T10235

TEXAS INSTR (LOGIC)

T-52-31

logic diagram (positive logic)



PRODUCT PREVIEW