

# Dual J-K Flip-Flop with Set and Reset

## High-Performance Silicon-Gate CMOS

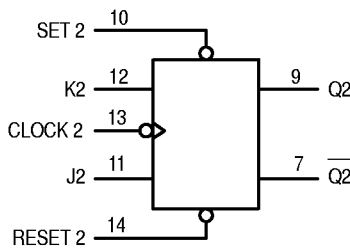
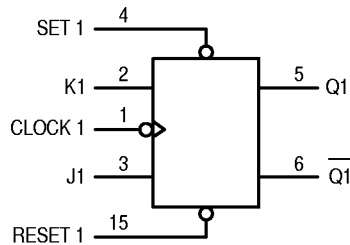
The MC74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC112 is identical in function to the HC76, but has a different pinout.

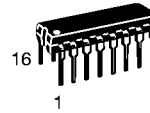
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates

### LOGIC DIAGRAM

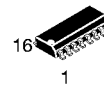


PIN 16 =  $V_{CC}$   
PIN 8 = GND

## MC74HC112



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**D SUFFIX**  
SOIC PACKAGE  
CASE 751B-05



**DT SUFFIX**  
TSSOP PACKAGE  
CASE 948F-01

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC74HCXXXD	SOIC
MC74HCXXXDT	TSSOP

### PIN ASSIGNMENT

CLOCK 1	1	16	$V_{CC}$
K1	2	15	RESET 1
J1	3	14	RESET 2
SET 1	4	13	CLOCK 2
Q1	5	12	K2
$\overline{Q1}$	6	11	J2
$\overline{Q2}$	7	10	SET 2
GND	8	9	Q2

### FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	$\sim$	L	L	No Change	
H	H	$\sim$	L	H	L	H
H	H	$\sim$	H	L	H	L
H	H	$\sim$	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	$\nearrow$	X	X	No Change	

\* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V	
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V	
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V	
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA	
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA	
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA	
P <sub>D</sub>	Power Dissipation in Still Air	Plastic DIP†	750	mW
		SOIC Package†	500	
		TSSOP Package†	450	
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP)	260	°C	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C  
 TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
			4.5	± 0.1	± 1.0	± 1.0	
			2.0	± 0.1	± 1.0	± 1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μA
			4.5	4	40	80	
			2.0	4	40	80	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or Q (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q or Q (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Set to Q or Q (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		35		

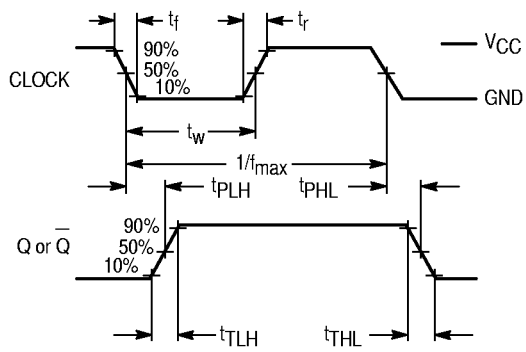
\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input  $t_r = t_f = 6$  ns)

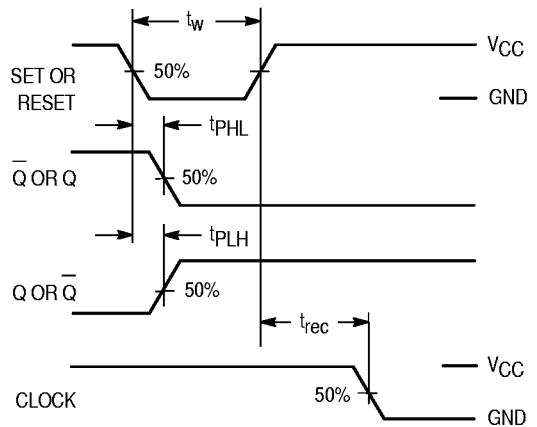
Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

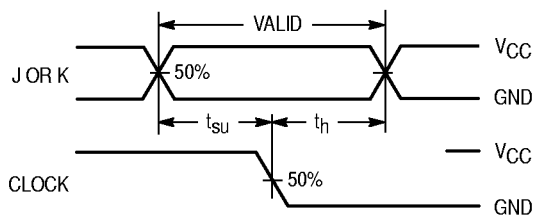
**SWITCHING WAVEFORMS**



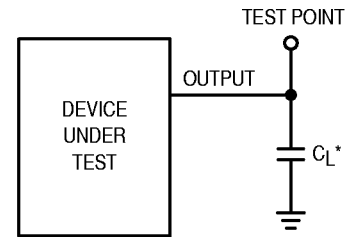
**Figure 1.**



**Figure 2.**



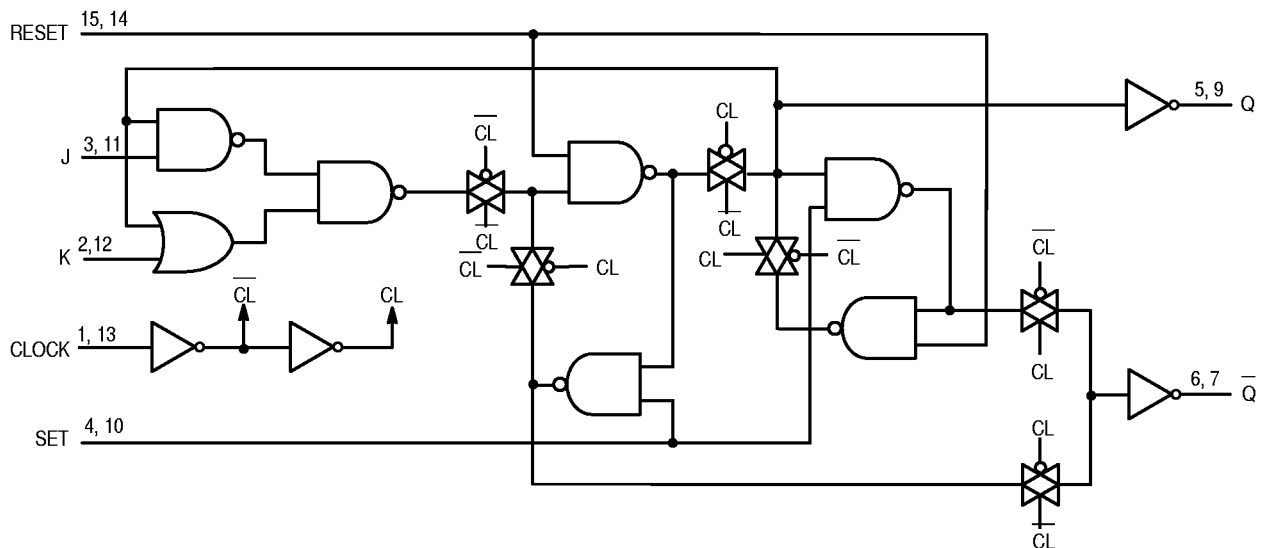
**Figure 3.**



\* Includes all probe and jig capacitance

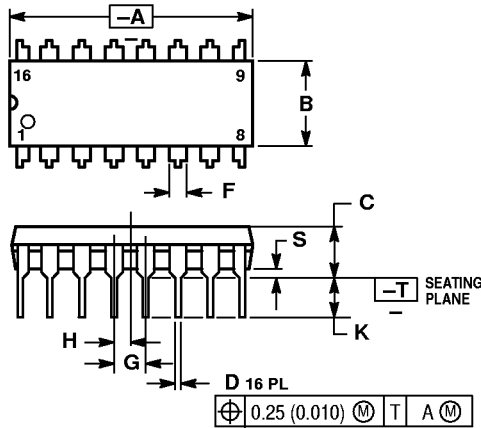
**Figure 4. Test Circuit**

**EXPANDED LOGIC DIAGRAM**



OUTLINE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**

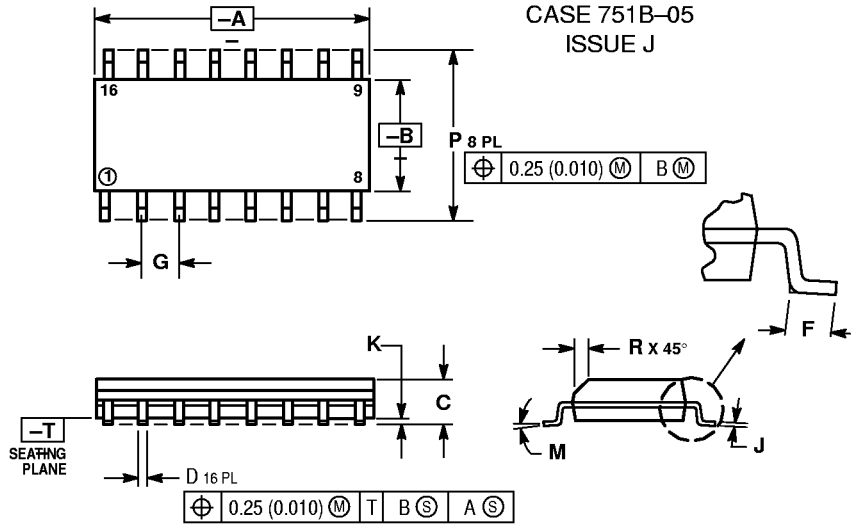


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751B-05**  
**ISSUE J**



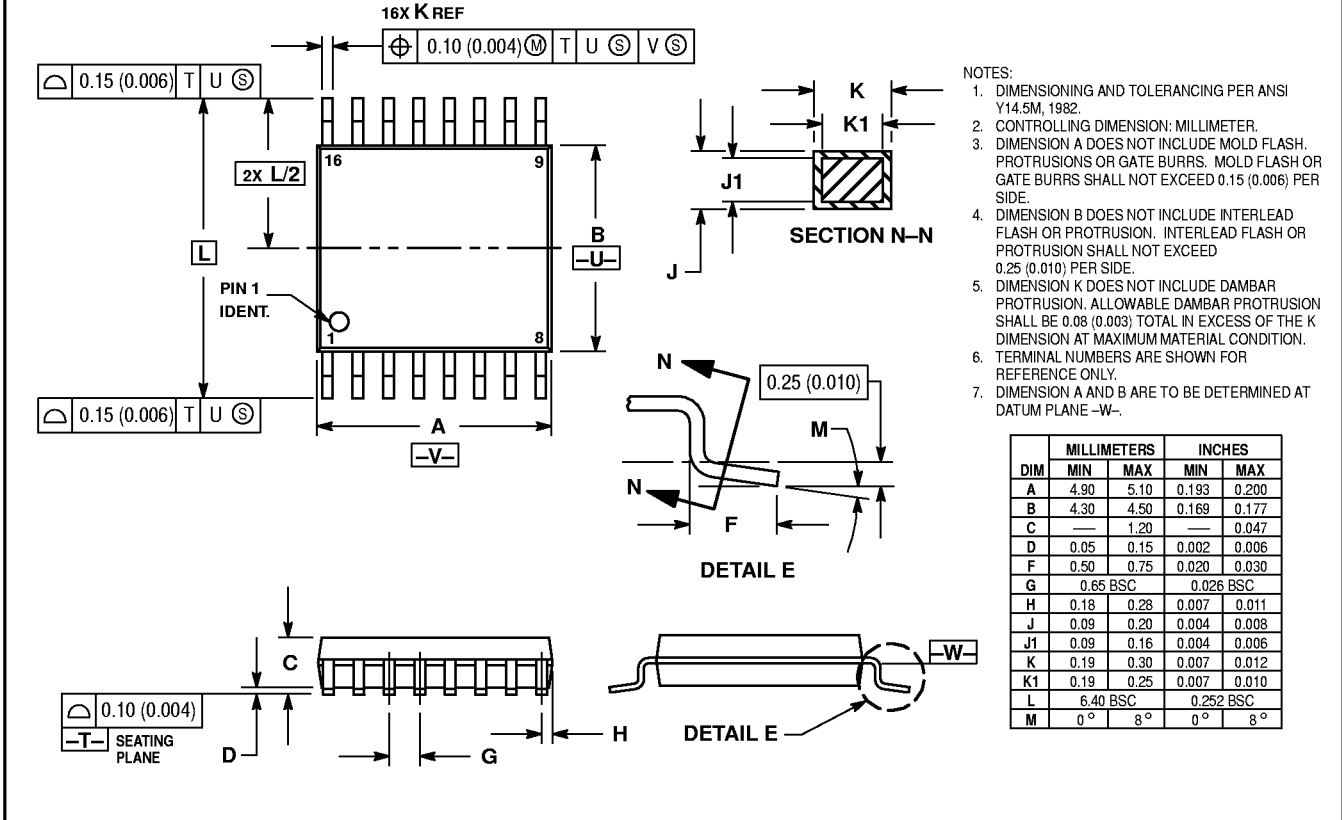
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948F-01  
 ISSUE O



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