

54ABT/74ABT273 Octal D-Type Flip-Flop

General Description

The 'ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'ABT377 for clock enable version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Military Drawing (SMD) 5962-9321701

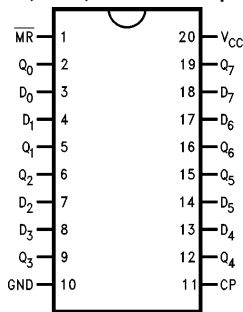
Commercial	Military	Package Number	Package Description
74ABT273CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT273CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54ABT273J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT273CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT273W/883	W20A	20-Lead Cerpack
	54ABT273E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT273CMTC (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, MSAX, and MTCX.

Note 2: Contact factory for package availability.

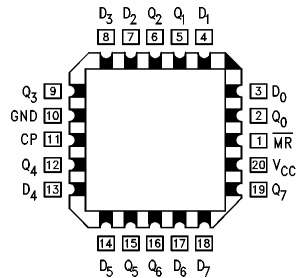
Connection Diagrams

Pin Assignment for
DIP, SOIC, SSOP and Flatpak



TL/F/11549-1

Pin Assignment
for LCC



TL/F/11549-2

Pin Names	Description
D ₀ –D ₇	Data Inputs
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ –Q ₇	Data Outputs

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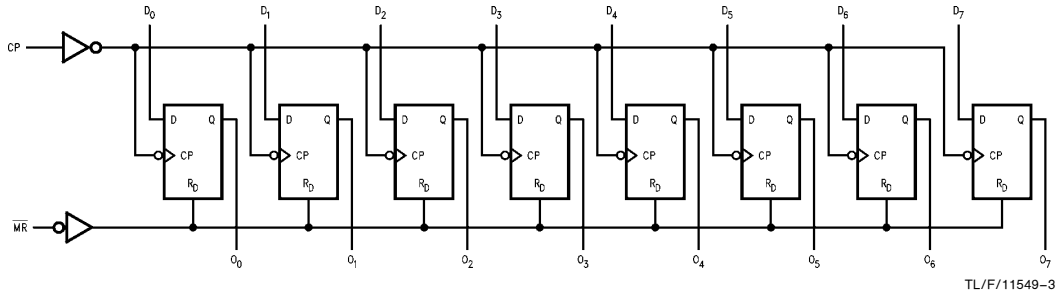
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	\overline{MR}	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↘	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
↗ = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to +4.75V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current (Across Comm Operating Range) -500 mA

Over Voltage Latchup V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT273			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT/74ABT 54ABT 74ABT	2.5 2.0 2.0		V	Min	I _{OH} = -3 mA I _{OH} = -24 mA I _{OH} = -32 mA
V _{OL}	Output LOW Voltage	54ABT 74ABT		0.55 0.55	V	Min	I _{OL} = 48 mA I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5 5	μA	Max	V _{IN} = 2.7V (Note 2) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-5 -5	μA	Max	V _{IN} = 0.5V (Note 2) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCT}	Maximum I _{CC} /Input Outputs Enabled			1.5	mA	Max	V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} No Load			0.3	mA/ MHz	Max	Outputs Open (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 2: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT		54ABT		74ABT		Units	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min		Max
f_{max}	Max Clock Frequency	150	200		150		150	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	2.0		6.0	1.0	7.0	2.0	6.0	ns
t_{PHL}	Propagation Delay MR to O_n	2.5		7.4	1.0	8.2	2.5	7.4	ns

AC Operating Requirements

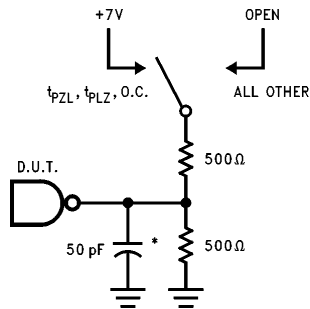
Symbol	Parameter	74ABT		54ABT		74ABT		Units	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_n to CP	2.0		2.0	2.0		2.0	2.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_n to CP	1.2		1.4	1.2		1.2	1.2	ns
$t_w(\text{H})$ $t_w(\text{L})$	Pulse Width, CP, HIGH or LOW	3.3		3.3	3.3		3.3	3.3	ns
$t_w(\text{L})$	Master Reset Pulse Width, LOW	3.3		3.3	3.3		3.3		ns
t_{REC}	Recovery Time MR to CP	2.0		2.0	2.0		2.0		ns

Capacitance (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 1)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

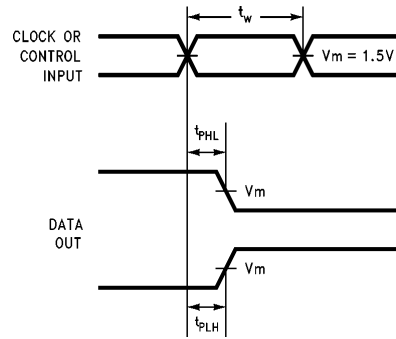
Note 1: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-833B, Method 3012.

AC Loading



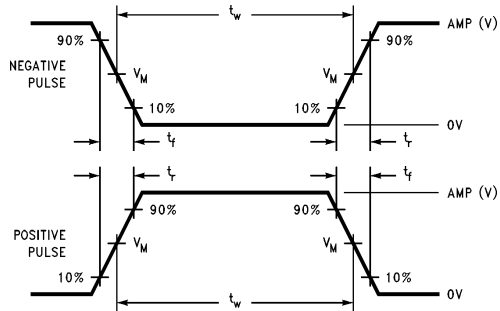
*Includes jig and probe capacitance TL/F/11549-4

FIGURE 1. Standard AC Test Load



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FIGURE 4. Propagation Delay, Pulse Width Waveforms



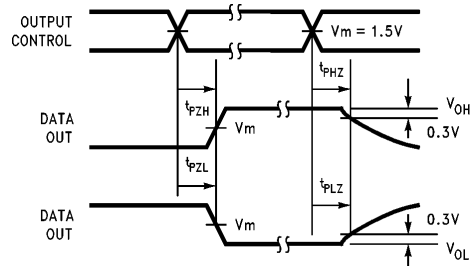
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FIGURE 2a. $V_M = 1.5V$

Input Pulse Requirements

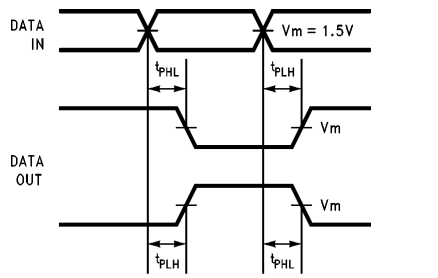
Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements



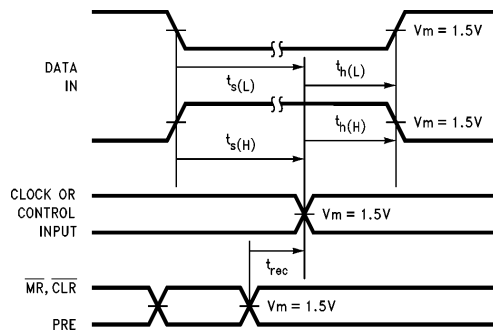
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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times



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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

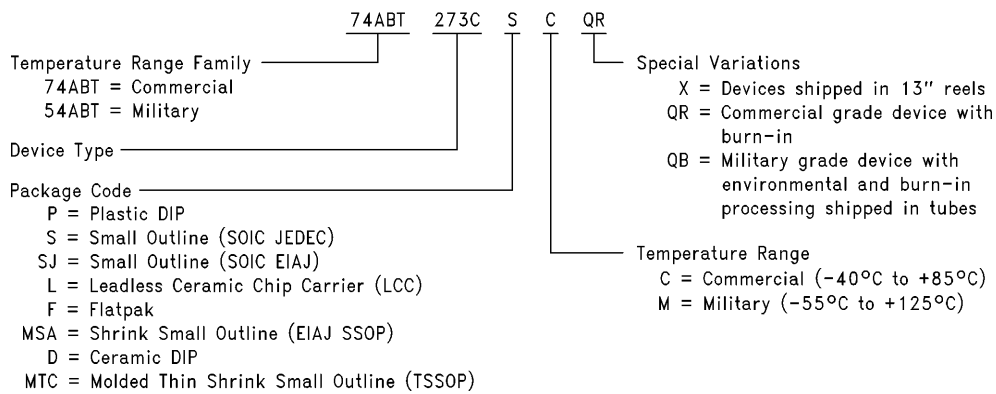


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FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

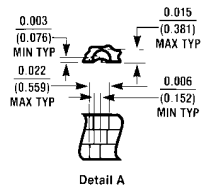
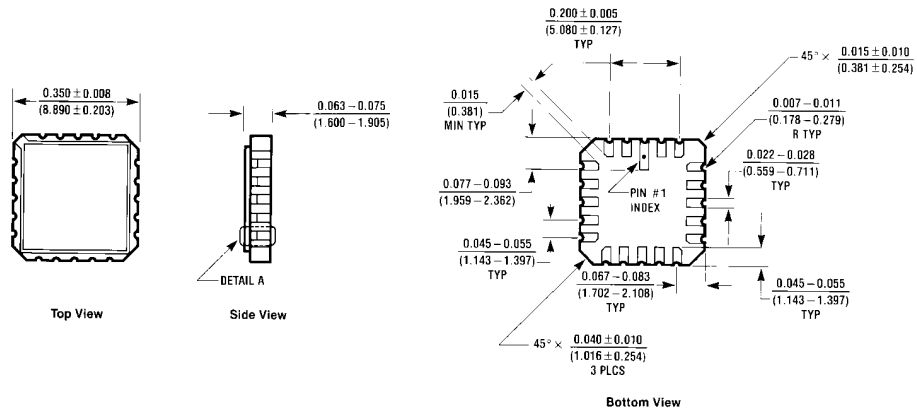
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



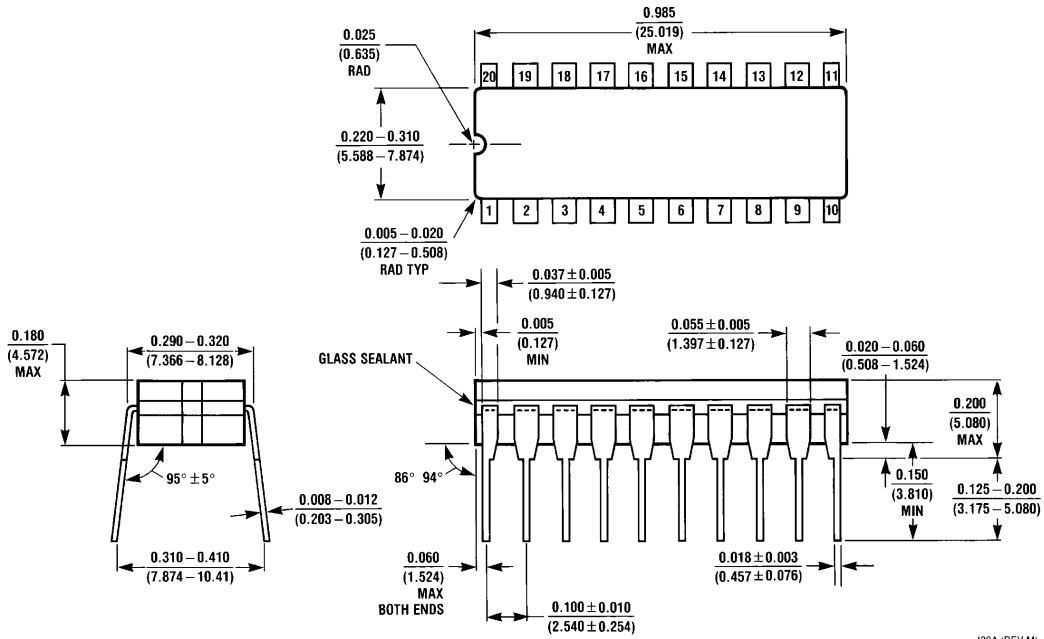
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Physical Dimensions inches (millimeters)



E20A (REV D)

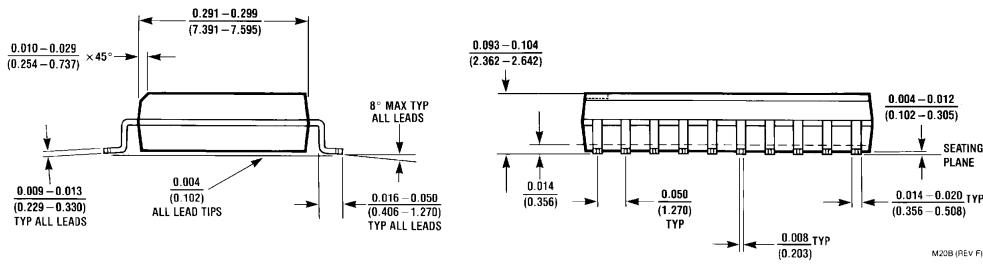
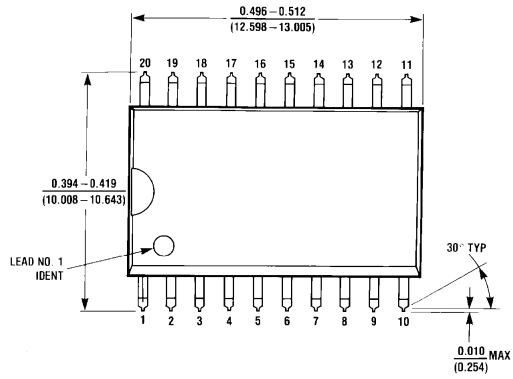
20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



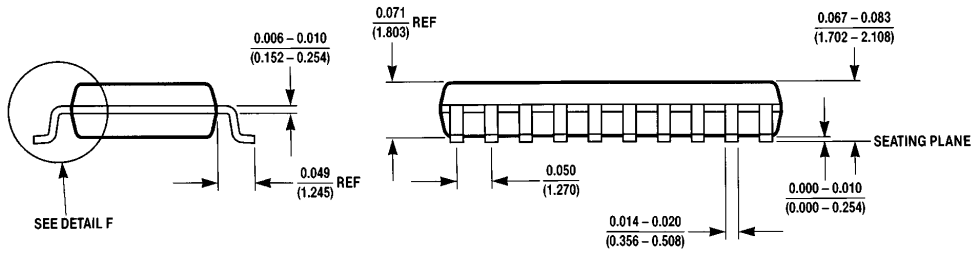
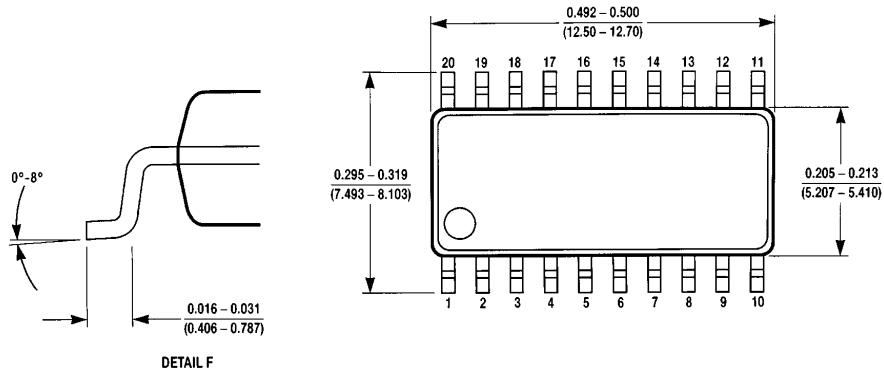
J20A (REV M)

20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

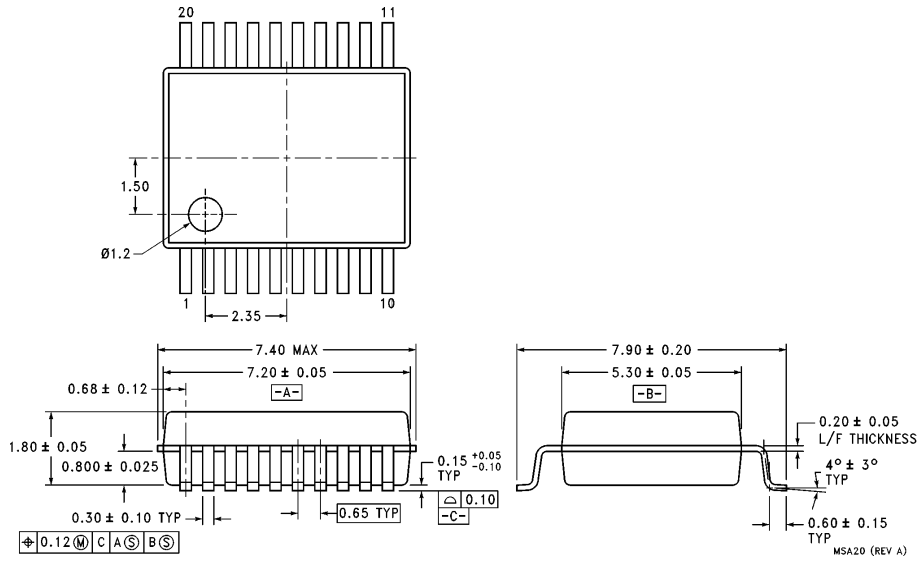


**20-Lead Small Outline Integrated Circuit JEDEC (S)
NS Package Number M20B**



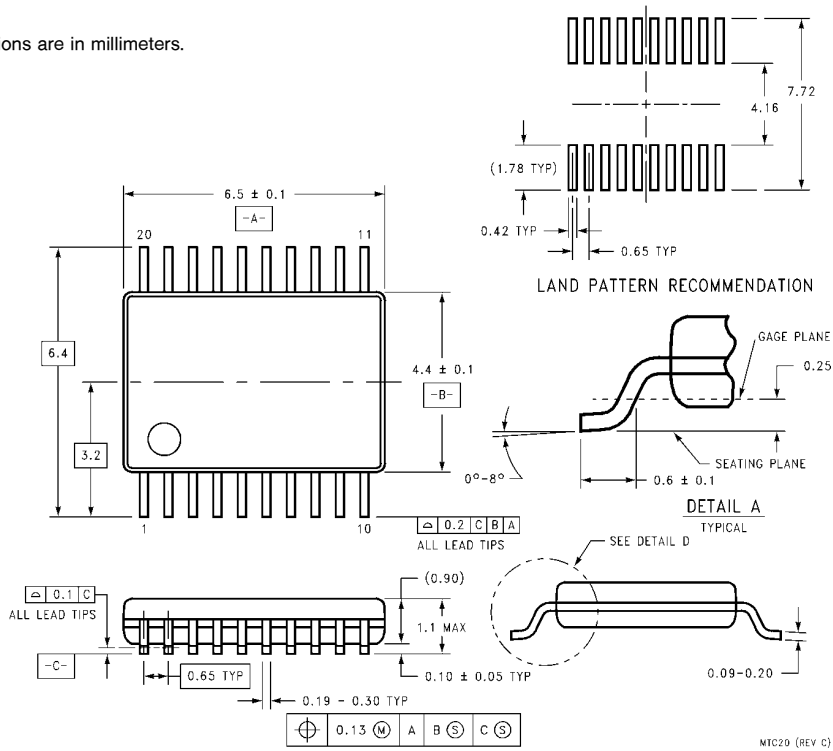
**20-Lead Small Outline Integrated Circuit EIAJ (SJ)
NS Package Number M20D**

Physical Dimensions inches (millimeters) (Continued)



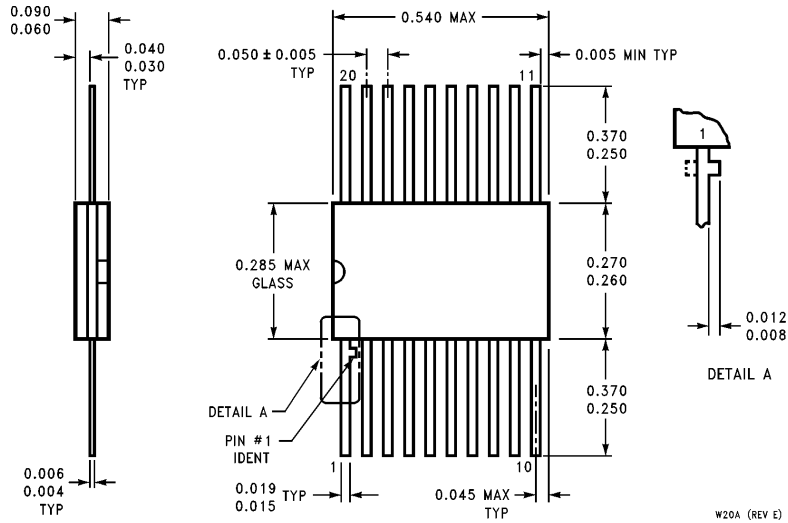
**20-Lead Plastic EIAJ SSOP (MSA)
NS Package Number MSA20**

All dimensions are in millimeters.



**20-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20**

Physical Dimensions inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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