

Dual octal D-type transparent latch; 3-state**74ALVC16373****FEATURES**

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no.8-1A
- CMOS low power consumption
- MultiByte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- 5 V to 3.3 V level shifting
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The 74ALVC16373 is a dual octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (LE) input and one output enable (OE) are provided for each octal.

The "16373" consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the eight latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

QUICK REFERENCE DATAGND = 0 V; T_{amb} = 25 °C; t_r = t_f = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	propagation delay D _n to Q _n ; LE to Q _n	C _L = 50 pF V _{CC} = 3.3 V	3.0 3.0	ns
C _I	input capacitance		3.0	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC15373DL	48	SSOP	plastic	SSOP48/SOT370

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q ₀ to 1Q ₇	'1Q' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V _{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q ₀ to 2Q ₇	'2Q' data inputs/outputs
24	$\overline{2OE}$	'2' output enable input (active LOW)
25	2LE	'2' latch enable
36, 35, 33, 32, 30, 29, 27, 26	2D ₀ to 2D ₇	'2D' data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D ₀ to 1D ₇	'1D' data inputs
48	1LE	'1' latch enable

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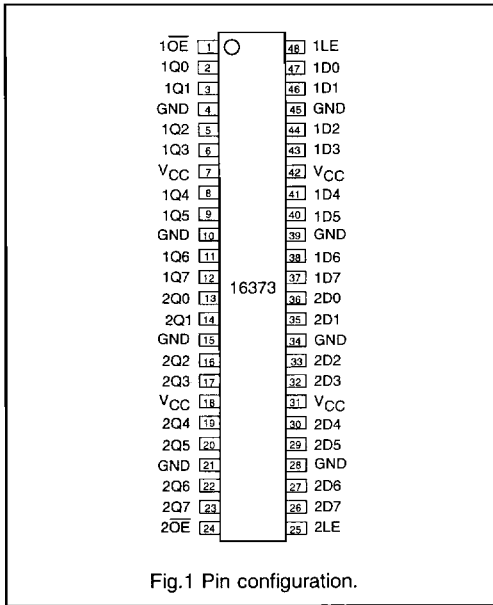


Fig.1 Pin configuration.

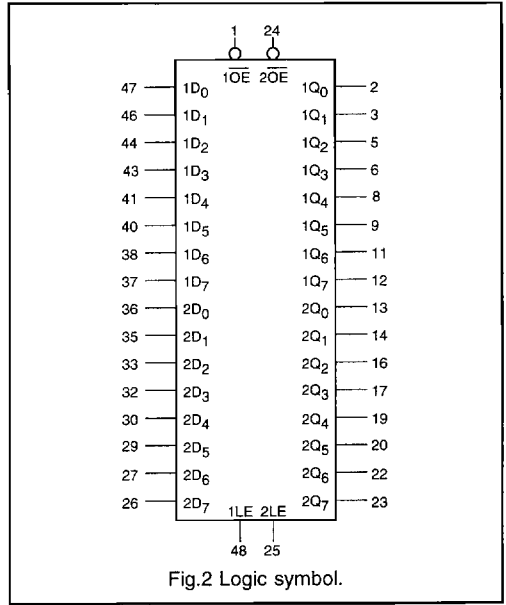


Fig.2 Logic symbol.

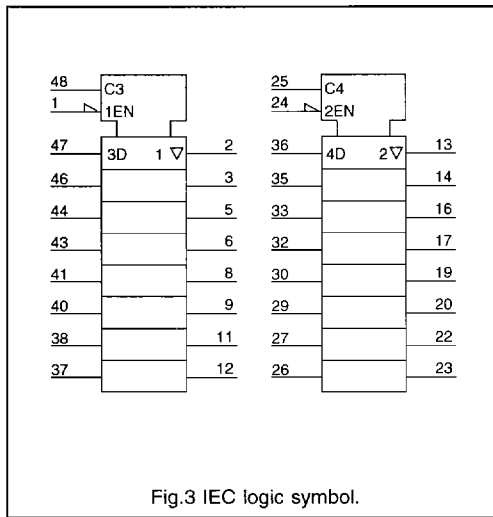


Fig.3 IEC logic symbol.

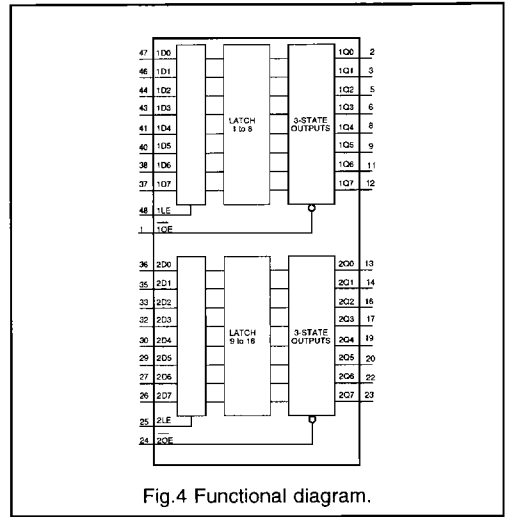
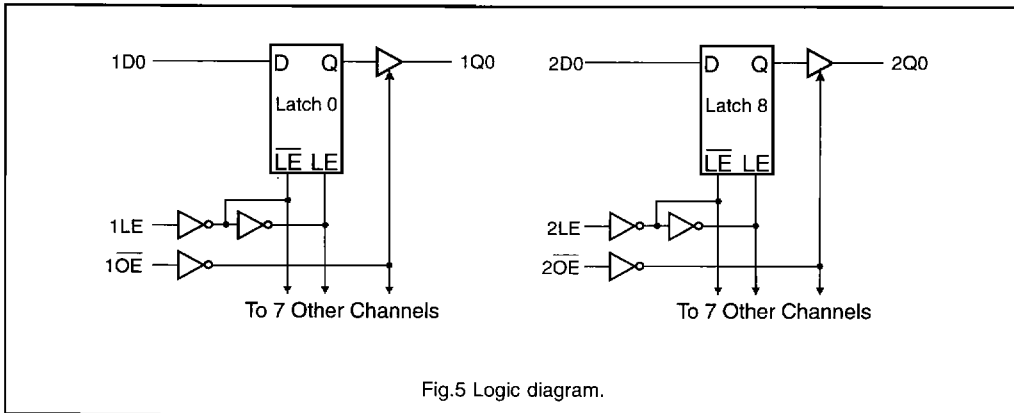


Fig.4 Functional diagram.

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FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	\overline{OE}	LE	D_n	Q_0 to Q_7
enable and read register (transparent mode)	L	H	L	L
	L	H	H	H
latch and read register	L	L	l	L
	L	L	h	H
latch register and disable outputs	H	X	X	Z

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
- X = don't care
- Z = high impedance OFF-state

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DC characteristics for 74ALVC16373

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

 I_{CC} category: MSI**AC characteristics for 74ALVC16373**GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF

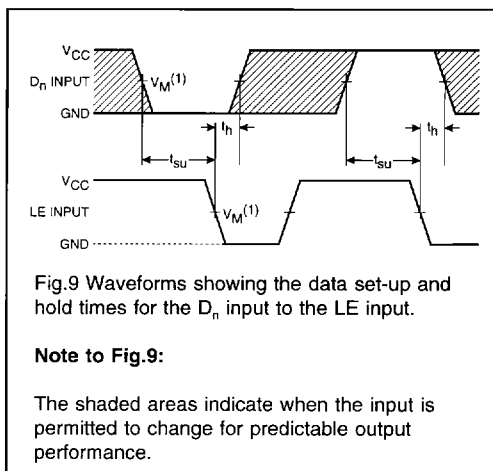
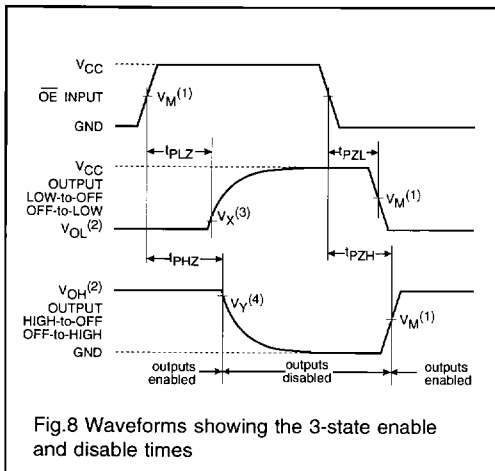
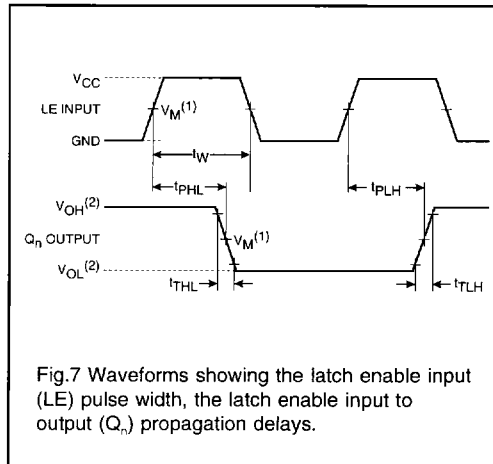
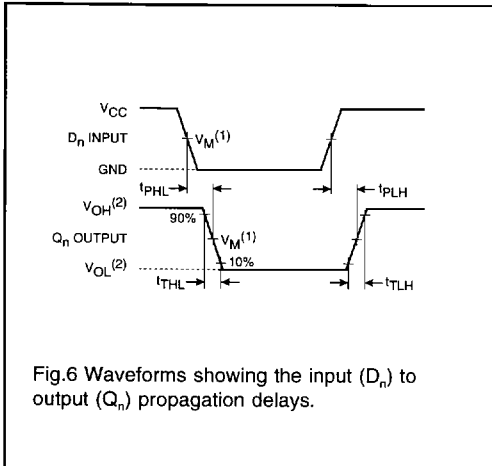
SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	-	-	17.6 4.8 3.0*	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	-	-	19.2 5.3 3.0*	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time OE to Q_n	-	-	20.0 5.5 5.0	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Q_n	-	-	20.2 5.6 5.1	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_w	LE pulse width HIGH	2.7 2.5	- -	- -	ns	2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time D_n to LE	2.2 0.7 0.6	- - -	- - -	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_h	hold time D_n to LE	2.2 0.7 0.6	- - -	- - -	ns	1.2 2.7 3.0 to 3.6	Fig.9

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS (per section of eight bits)



Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$