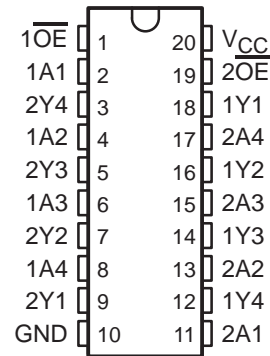


SN74LVCZ244A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES274B – JUNE 1999 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Shrink Small-Outline (DB), Plastic Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ244A is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

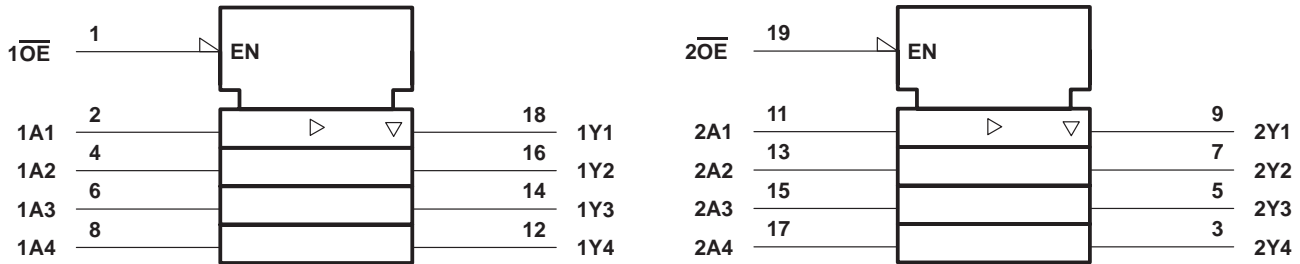
SN74LVCZ244A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES274B – JUNE 1999 – REVISED JANUARY 2000

FUNCTION TABLE
(each buffer)

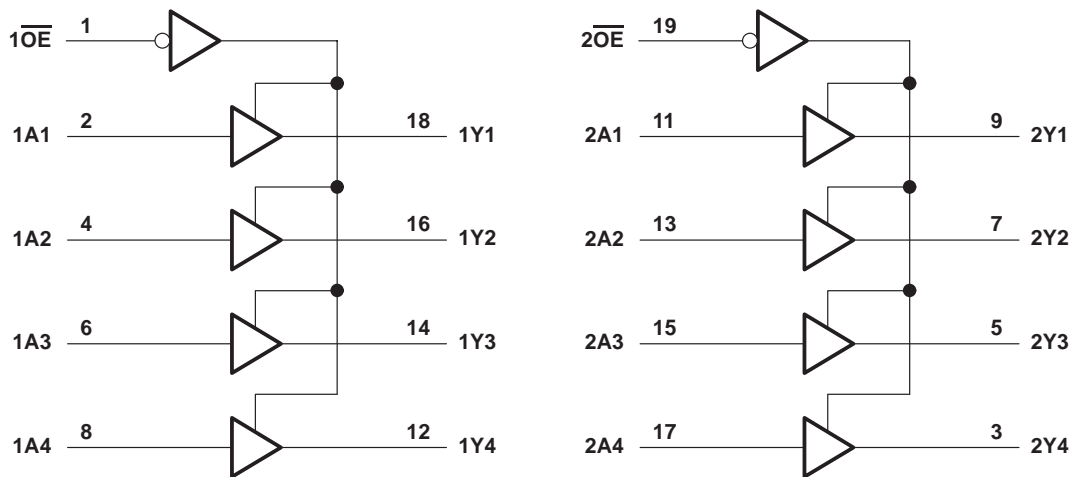
INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVCZ244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES274B – JUNE 1999 – REVISED JANUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}
		3-state	0	5.5
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	–12	
		$V_{CC} = 3$ V	–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	6		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	150		µs/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVCZ244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCES274B – JUNE 1999 – REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	μA
I _{off}	V _O = 0 to 5.5 V	0			±5	μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±5	μA
I _{OZPU}	V _O = 0.5 V to 2.5 V, \overline{OE} = don't care	0 to 1.5 V			±5	μA
I _{OZPD}	V _O = 0.5 V to 2.5 V, \overline{OE} = don't care	1.5 V to 0			±5	μA
I _{CC}	V _I = V _{CC} or GND	3.6 V			100	μA
	3.6 V ≤ V _I ≤ 5.5 V‡		I _O = 0		100	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			100	μA
C _i	V _I = V _{CC} or GND	3.3 V	3.5			pF
C _o	V _O = V _{CC} or GND	3.3 V	5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

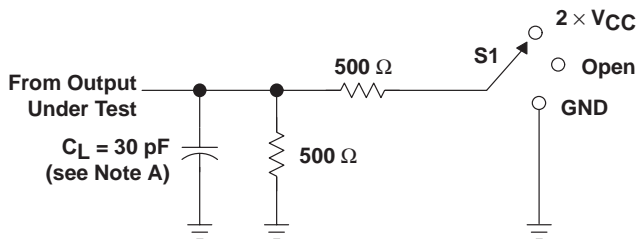
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A		6.9	1.5	5.9	ns
t _{en}	\overline{OE}	A or B		8.6	1.5	7.6	ns
t _{dis}	\overline{OE}	A or B		6.8	1.5	6.5	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 3.3 V	UNIT
			TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	40	pF
		Outputs disabled	3	

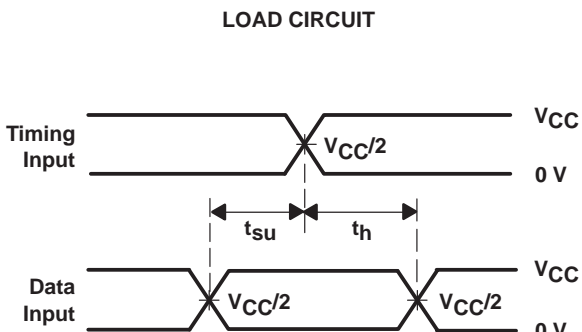


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

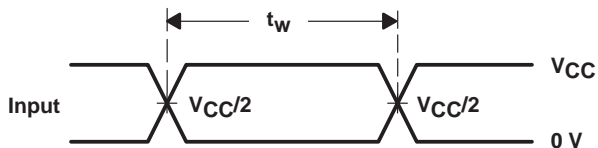


LOAD CIRCUIT

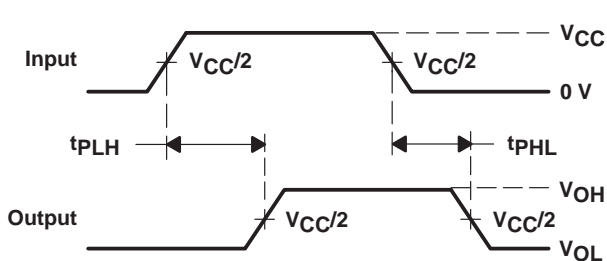
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



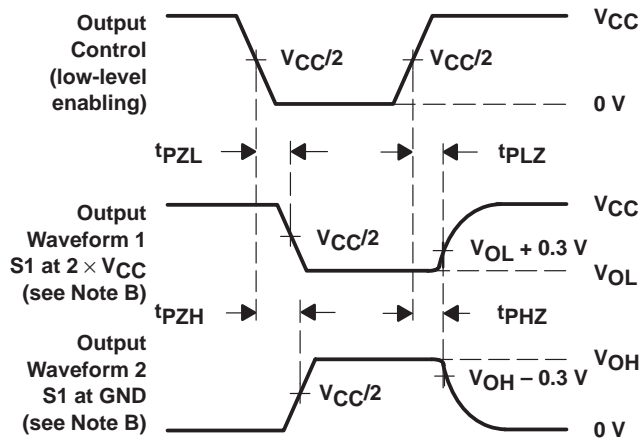
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

TEXAS INSTRUMENTS THE WORLD LEADER IN DSP AND ANALOG

Products [GO] Development Tools [GO] Applications [GO]

Search [GO]
 Advanced Search
 TI Home
 TI&ME
 Employment
 Tech Support
 Comments
 Site Map
 TI Global

PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY](#) | [SAMPLES](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LVCZ244A, Octal Buffer/Driver With 3-State Outputs

DEVICE STATUS: **ACTIVE**

FEATURES

[▲ Back to Top](#)

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Shrink Small-Outline (DB), Plastic Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

EPIC is a trademark of Texas Instruments Incorporated.

DESCRIPTION

[▲ Back to Top](#)

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ244A is organized as two 4-bit line drivers with separate output-enable (OE\) inputs. When OE\ is low, the device passes data from the A inputs to the Y outputs. When OE\ is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ244A is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

[▲ Back to Top](#)

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

[▲ Back to Top](#)

Full datasheet in Acrobat PDF: [sces274b.pdf](#) (83 KB) (Updated: 01/04/2000)

Full datasheet in Zipped PostScript: [sces274b.psz](#) (88 KB)

APPLICATION NOTES

[▲ Back to Top](#)

View Application Reports for [Digital Logic](#)

- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs](#) (SCBA012A - Updated: 08/01/1997)
- [CMOS Power Consumption and CPD Calculation](#) (SCAA035B - Updated: 06/01/1997)
- [Implications of Slow or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVC Characterization Information](#) (SCBA011 - Updated: 12/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Low-Voltage Logic \(LVC\) Designer's Guide](#) (SCBA010 - Updated: 09/01/1996)
- [Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices](#) (SCEA005 - Updated: 12/01/1997)
- [Timing Differences Of 10-pF Versus 50pF Loading](#) (SCEA004 - Updated: 11/01/1996)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS

[▲ Back to Top](#)

- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 4 KB - Updated: 05/06/1999)
- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

SAMPLES

[▲ Back to Top](#)

<u>ORDERABLE DEVICE</u>	<u>PACKAGE</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	<u>SAMPLES</u>
SN74LVCZ244ADBR	<u>DB</u>	20	-40 TO 85	ACTIVE	Request Samples
SN74LVCZ244ADWR	<u>DW</u>	20	-40 TO 85	ACTIVE	Request Samples
SN74LVCZ244APWR	<u>PW</u>	20	-40 TO 85	ACTIVE	Request Samples

PRICING/AVAILABILITY

[▲ Back to Top](#)

<u>ORDERABLE DEVICE</u>	<u>PACKAGE</u>	<u>PINS</u>	<u>TEMP</u> <u>(°C)</u>	<u>STATUS</u>	<u>BUDGETARY</u> <u>PRICE</u> <u>US\$/UNIT</u> <u>QTY=1000+</u>	<u>PACK</u> <u>QTY</u>	<u>PRICING/AVAILABILITY</u>
SN74LVCZ244ADBR	<u>DB</u>	20	-40 TO 85	ACTIVE	0.59	2000	<u>Check stock or order</u>
SN74LVCZ244ADW	<u>DW</u>	20	-40 TO 85	ACTIVE	0.59	25	<u>Check stock or order</u>
SN74LVCZ244ADWR	<u>DW</u>	20	-40 TO 85	ACTIVE	0.59	2000	<u>Check stock or order</u>
SN74LVCZ244AN	<u>N</u>	20	-40 TO 85	ACTIVE		20	<u>Check stock or order</u>
SN74LVCZ244ANSR	<u>NS</u>	20	-40 TO 85	OBSOLETE			
SN74LVCZ244APW	<u>PW</u>	20	-40 TO 85	OBSOLETE			
SN74LVCZ244APWR	<u>PW</u>	20	-40 TO 85	ACTIVE	0.59	2000	<u>Check stock or order</u>

Table Data Updated on: 11/17/2000

© Copyright 2000 Texas Instruments Incorporated. All rights reserved. [Trademarks](#) | [Privacy Policy](#)
| [Important Notice](#)