3-to-8 Line Decoder/Latch

The TC74HC137A is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

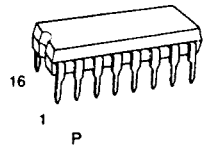
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is composed of 3-bit input register with a common $\overline{GL}$ enable input and a 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of the outputs will go low. When the enable input G1 is held low or $\overline{G2}$ is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application of address decoder for memory system.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: f_{pd} = 17ns(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: $V_{CC(opr)}$ = 2V ~ 6V
- Pin and Function Compatible with 74LS137



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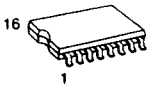

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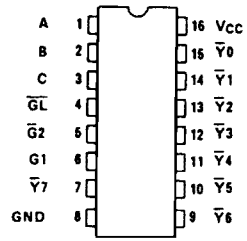
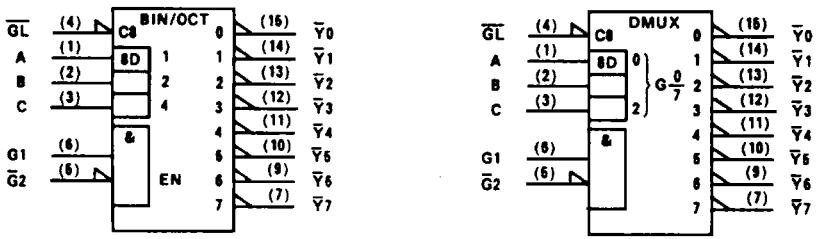


(TOP VIEW)

Pin Assignment

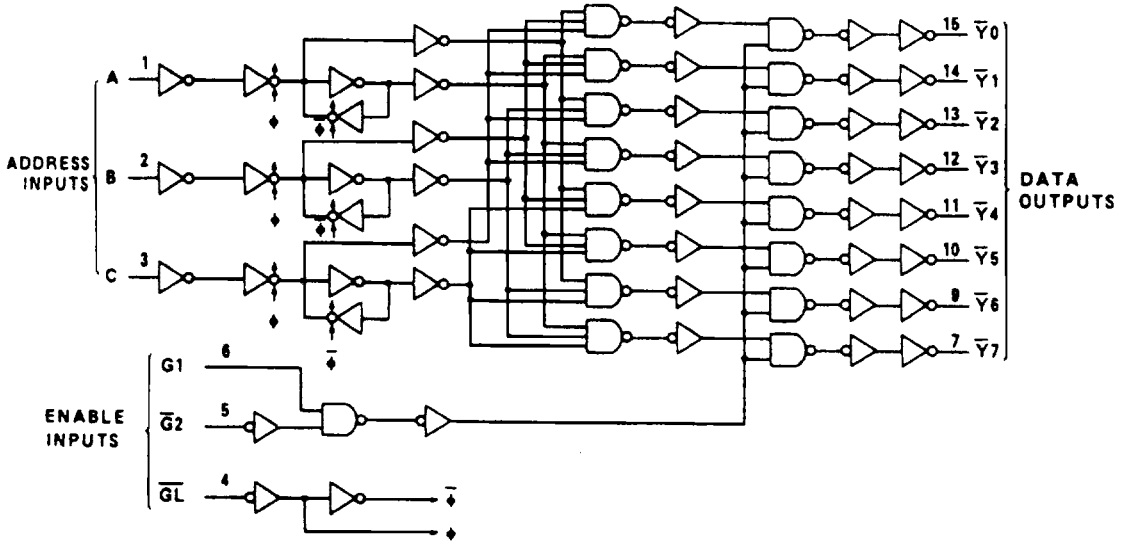


IEC Logic Symbol

Truth Table

Input						Output								Selected Output
Enable			Address											
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
L	L	H	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}0$
L	L	H	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}1$
L	L	H	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}2$
L	L	H	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}3$
L	L	H	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}4$
L	L	H	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}5$
L	L	H	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}6$
L	L	H	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}7$
H	L	H	X	X	X	OUTPUTS are latched at the time when $\overline{GL}$ is taken High level								

X: Don't Care



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
				V_{CC}	Min	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	–	4.13 5.63	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	–	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$ $t_{W(H)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (A, B, C-$\overline{GL}$)	t_s	–	2.0	–	50	65	
			4.5	–	10	13	
			6.0	–	9	11	
Minimum Hold Time (A, B, C-$\overline{GL}$)	t_h	–	2.0	–	25	30	
			4.5	–	5	6	
			6.0	–	5	5	

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

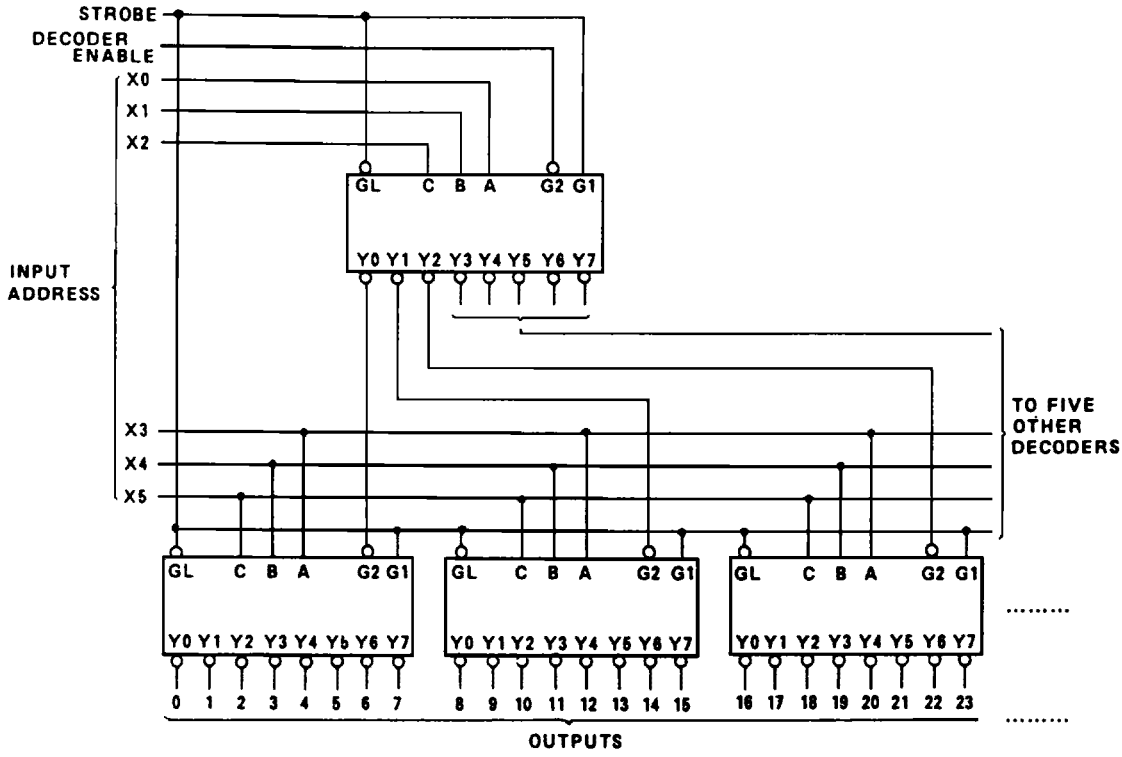
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}	–	–	11	19	
Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	t_{pLH} t_{pHL}	–	–	12	19	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH} t_{pHL}	–	–	18	29	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}	–	–	17	28	

AC Electrical Characteristics ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}	–	2.0	–	45	115	–	145	
			4.5	–	14	23	–	29	
			6.0	–	12	20	–	25	
Propagation Delay Time (G2 - $\overline{Y}$)	t_{pLH} t_{pHL}	–	2.0	–	50	115	–	145	
			4.5	–	15	23	–	29	
			6.0	–	13	20	–	25	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH} t_{pHL}	–	2.0	–	70	170	–	215	
			4.5	–	22	34	–	43	
			6.0	–	19	29	–	37	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}	–	2.0	–	70	165	–	205	
			4.5	–	21	22	–	41	
			6.0	–	18	28	–	35	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	56	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$



6 Line to 64 Line Decoder with Input Address Storage

Typical Application

Notes