



High-Speed CMOS Quad 2 Input Multiplexers

QS54/74FCT157T
QS54/74FCT158T
QS54/74FCT257T
QS54/74FCT258T

QS54/74FCT2157T
QS54/74FCT2158T
QS54/74FCT2257T
QS54/74FCT2258T

FEATURES/BENEFITS

- Pin and function compatible to the 74F1/257/8 74FCT 1/257/8 and 74FCT1/257/8T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 157T, 158T, 257T, 258T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 4.3 ns for C
- I_{OL} = 48 mA Com., 32 mA Mil.

FCT-T 2157T, 2158T, 2257T, 2258T

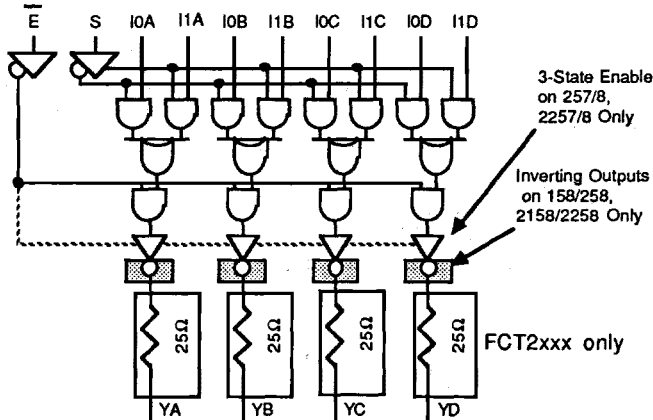
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and C speed grades with 4.3 ns for C
- I_{OL} = 12mA Com.

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DESCRIPTION

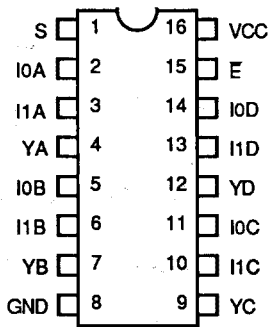
The QSFCT157/8T and QSFCT257/8T are high speed CMOS TTL-compatible 8-input multiplexers. The 157/257 parts are non-inverting; the 158/258 are inverting. The 157/8 has TTL outputs; the 257/8 has 3-state outputs. The QSFCT2157/8T and QSFCT2257/8T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

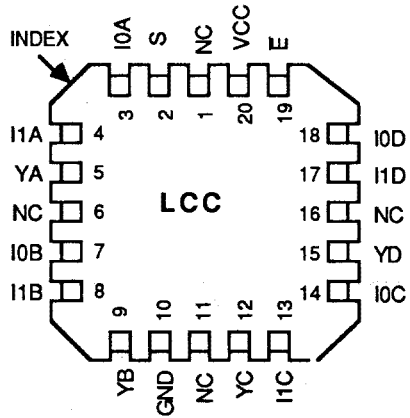
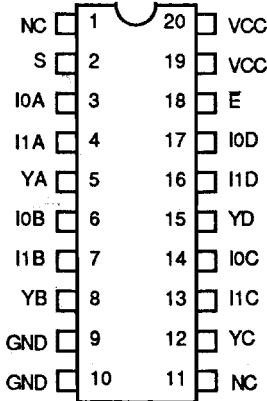


PIN CONFIGURATIONS

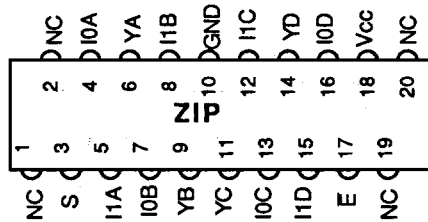
DIP, SOIC, QSOP



HQSOP



ALL PINS TOP



Note: Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

FUNCTION TABLES

E	S	157				158				Function
		YA	YB	YC	YD	YA	YB	YC	YD	
H	X	L	L	L	L	H	H	H	H	Disable
L	L	I0A	I0B	I0C	I0D	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	I1A	I1B	I1C	I1D	Select 1

E	S	257				258				Function
		YA	YB	YC	YD	YA	YB	YC	YD	
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	I0A	I0B	I0C	I0D	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	I1A	I1B	I1C	I1D	Select 1

PIN DESCRIPTION

Name	I/O	Description
Ixx	I	Data Inputs
S	I	Select Input
E	I	Enable Input
YA-YD	O	Data Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
 DC Output Voltage V_O -0.5V to 7.0V
 DC Input Voltage V_I -0.5V to 7.0V
 AC Input Voltage (for a pulse width ≤ 20 ns)..... -3.0V
 DC Input Diode Current with $V_I < 0$ -20 mA
 DC Output Diode Current with $V_O < 0$ -50 mA
 DC Output Current Max. sink current/pin..... 120 mA
 Maximum Power Dissipation..... 0.5 watts
 T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-3,5,6,10,11,13-15	4	4	5	7	pF
4,7,9,12	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{thl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$		-	-	5	
Ios	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$		-60	-	-225	mA
Ior	Current Drive FCT2XXX	$V_{CC} = \text{Min}, V_o = 2.0\text{V} (3)$		50	-	-	mA
Vic	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	loh = 12 mA (MIL)	2.4	-	-	Volts
			loh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	lol = 32 mA (MIL)	-	-	0.50	
			lol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	-	0.50	
			lol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	25	-	Ω
			lol = 12 mA (COM)	20	28	40	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i=3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	157/8 257/8 2157/8 2257/8		157/8A 257/8A 2157/8A 2257/8A		157/8C 257/8C 2157/8C 2257/8C		Unit
			Min	Max	Min	Max	Min	Max	
t IY	Propagation Delay In to Y, 157/8/257/8	COM	1.5	6.0	1.5	5.0	1.5	4.3	ns
		MIL	1.5	7.0	1.5	5.8	1.5	5.0	
	Propagation Delay In to Y, 2157/8/2257/8	COM	1.5	6.0	1.5	5.0	1.5	4.3	
		MIL	1.5	7.0	1.5	5.8	1.5	5.0	
t SY	Propagation Delay S to Y, 157/8/257/8	COM	1.5	10.5	1.5	7.0	1.5	5.2	
		MIL	1.5	12	1.5	8.1	1.5	6.0	
	Propagation Delay S to Y, 2157/8/2257/8	COM	1.5	10.5	1.5	7.0	1.5	5.2	
		MIL	1.5	12	1.5	8.1	1.5	6.0	
t OEH t OEL	Output Enable Time E to Yi, 157/8	COM	1.5	10.5	1.5	6.0	1.5	4.8	
		MIL	1.5	12	1.5	7.4	1.5	5.9	
	Output Enable Time E to Yi, 2157/8	COM	1.5	10.5	1.5	6.0	1.5	4.8	
		MIL	1.5	12	1.5	7.4	1.5	5.9	
t PZH t PZL	Output Enable Time E to Yi, 257/8	COM	1.5	8.5	1.5	7.0	1.5	6.0	
		MIL	1.5	10	1.5	8.0	1.5	6.8	
	Output Enable Time E to Yi, 2257/8	COM	1.5	8.5	1.5	7.0	1.5	6.0	
		MIL	1.5	10	1.5	8.0	1.5	6.8	
t PHZ t PLZ	Output Disable Time E to Yi, 257/8/2257/8	COM	2	1.5	6.0	1.5	5.5	1.5	5.0
		MIL	2	1.5	8.0	1.5	5.8	1.5	5.3

Notes:

- 1) Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) See Test Circuit and Waveforms.