REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R168-96.	96-08-01	R. MONNIN
B	Make changes to boilerplate and add device class T. - ro	98-12-04	R. MONNIN
C	Drawing updated to reflect current requirements. – gt	03-01-06	R. MONNIN

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
SANDRA ROONEY

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
95-11-09

MICROCIRCUIT, LINEAR RADIATION HARDENED CMOS, DUAL SPDT ANALOG SWITCHES, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-95813**

SHEET 1 OF 23

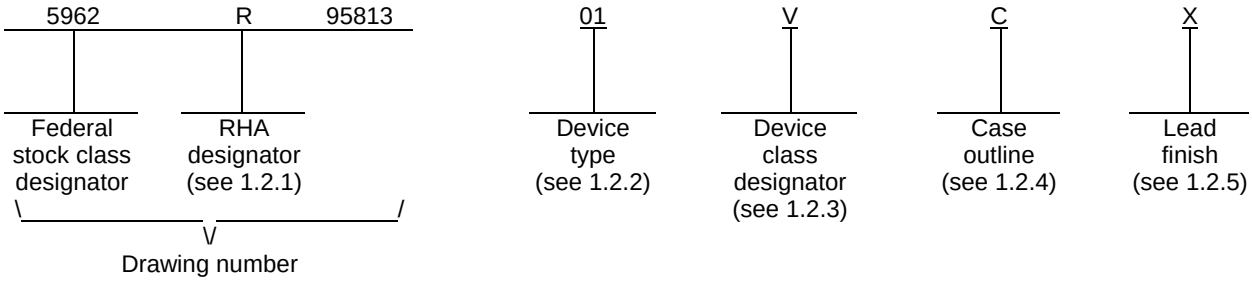
DSCC FORM 2233
APR 97

5962-E493-02

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS303RH	Radiation hardened DI, dual SPDT CMOS switch
02	HS307RH	Radiation hardened DI, dual SPDT CMOS switch
03	HS390RH	Radiation hardened DI, dual SPDT CMOS switch

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	CDIP2-T14	14	Dual-in-line
E	CDIP2-T16	16	Dual-in-line
X	CDFP3-F14	14	Flat package
Y	CDFP4-F16	16	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage between +V and -V ..... 44 V
Supply voltage between +V and ground ..... 22 V
Supply voltage between -V and ground ..... 22 V
Digital input overvoltage :
$+V_A$ ..... $+V_{SUPPLY}$ + 4 V
$-V_A$ ..... $-V_{SUPPLY}$ - 4 V
Analog input overvoltage :
$+V_S$ ..... $+V_{SUPPLY}$ + 1.5 V
$-V_S$ ..... $-V_{SUPPLY}$ - 1.5 V
Continuous current, S or D ..... 10 mA
Peak current, S or D
(pulsed at 1 ms, 10 percent duty cycle max) ..... 40 mA
Storage temperature range ..... -65°C to +150°C
Maximum package power dissipation at 125°C (P_D) 2/:
Case outlines C and E ..... 0.71 W
Case outlines X and Y ..... 0.48 W
Thermal resistance, junction-to-case (θ_{JC}):
Case outlines C and E ..... 19°C/W
Case outlines X and Y ..... 17°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
Case outlines C and E ..... 70°C/W
Case outlines X and Y ..... 105°C/W
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Operating supply voltage ($\pm V_{SUPPLY}$) ..... ±15 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.5 Radiation features

Dose rate upset (20 ns pulse) 3/
Maximum total dose available (dose rate = 50 – 300 rads(si)/s) ..... > 100 Krads (Si)
Latch-up 4/ ..... None

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capacity, provide heat sink or derate linearly (the derating is based on θ_{JA}) at the following rates:
Case outlines C and E ..... 14.3 mW/°C
Case outlines X and Y ..... 9.5 mW/°C
3/ Values to be specified when testing is completed.
4/ Guaranteed by process or design, not tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 82 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
"Switch on" resistance	$+R_{DS}$	V_D = 10 V, I_S = -10 mA	1	All		50	Ω
		S1/S2/S3/S4	2,3			75	
		M,D,P,L,R 2/	1			60	
	$-R_{DS}$	V_D = -10 V, I_S = 10 mA	1			50	
		S1/S2/S3/S4	2,3			75	
		M,D,P,L,R 2/	1			60	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +14 V, V_D = -14 V	1	All	-2	+2	nA
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
	$-I_{S(OFF)}$	V_S = -14 V, V_D = +14 V	1		-2	+2	
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = -14 V, V_S = +14 V	1	All	-2	+2	nA
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
	$-I_{D(OFF)}$	V_D = +14 V, V_S = -14 V	1		-2	+2	
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
Leakage current from an "ON" driver into the switch (Drain and Source)	$+I_{D(ON)}$	$V_D = V_S$ = +14 V	1	All	-2	+2	nA
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
	$-I_{D(ON)}$	$V_D = V_S$ = -14 V	1		-2	+2	
		S1/S2/S3/S4	2,3		-100	+100	
		M,D,P,L,R 2/	1		-100	+100	
Low level input address current	IAL	All channels V_A = 0.8 V	1,2,3	01,03	-1	+1	µA
		M,D,P,L,R 2/	1		-1	+1	
		All channels V_A = 3.5 V	1,2,3	02	-1	+1	
		M,D,P,L,R 2/	1		-1	+1	
High level input address current	I_{AH}	All channels V_A = 4.0 V	1,2,3	01,03	-1	+1	µA
		M,D,P,L,R 2/	1		-1	+1	
		All channels V_A = 11 V	1,2,3	02	-1	+1	
		M,D,P,L,R 2/	1		-1	+1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive supply current	+I	All channels V_A = 0.8 V	1	01,03		10	µA
			2,3			100	
		M,D,P,L,R 2/	1			100	
		V_{A1} = 0 V, V_{A2} = 4.0 V	1			0.5	mA
		V_{A1} = 4.0 V, V_{A2} = 0 V	2,3			1	
		M,D,P,L,R 2/	1			1	
		All channels V_A = 0 V, 15 V	1	02		10	µA
			2,3			100	
		M,D,P,L,R 2/, All channels V_A = 0 V	1			100	
		M,D,P,L,R 2/, All channels V_A = 15 V	1			100	
Negative supply current	-I	All channels V_A = 0.8 V	1	01,03		-10	µA
			2,3			-100	
		M,D,P,L,R 2/	1			-100	
		V_{A1} = 0 V, V_{A2} = 4.0 V	1			-10	
		V_{A1} = 4.0 V, V_{A2} = 0 V	2,3			-100	
		M,D,P,L,R 2/	1			-100	
		All channels V_A = 0 V, 15 V	1			-10	
			2,3			-100	
		M,D,P,L,R 2/	1			-100	
Switch input capacitance	$C_{IS(OFF)}$	Measured Source to 3/ 4/ GND	4	All		28	pF
Driver input capacitance	C_{C1}	V_A = 0 V 3/ 4/	4	All		10	pF
	C_{C2}	V_A = 15 V 3/ 4/				10	
Switch output	C_{OS}	Measured Drain to 3/ 4/ GND	4	All		28	pF
Off isolation	V_{ISO}	V_{GEN} = 1 V_{PP}, 3/ 4/ f = 1 MHz	4	All	40		dB
Cross talk	VCR	V_{GEN} = 1 V_{PP}, 3/ 4/ f = 1 MHz	4	All	40		dB
Charge transfer error	V_{CTE}	V_S = GND, 3/ 4/ C_L = 0.01 µF	4	All		15	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Break-before-make time delay	t_{OPEN}	R_L = 300 Ω, V_S = +3 V	9	01,03	30	150	ns
		V_{AH} = 5.0 V, V_{AL} = 0 V	10,11			300	
		See figure 3. M,D,P,L,R 2/	9		2	300	
		R_L = 300 Ω, V_S = +3 V	9	02	30	50	
		V_{AH} = 15.0 V, V_{AL} = 0 V	10,11			300	
		See figure 3. M,D,P,L,R 2/	9		2	300	
Switch turn “ON” time	t_{ON}	R_L = 300 Ω, V_S = +3 V	9	01,03		300	ns
		V_{AH} = 4.0 V, V_{AL} = 0 V	10,11			500	
		See figure 3. M,D,P,L,R 2/	9			500	
		R_L = 300 Ω, V_S = +3 V	9	02		300	
		V_{AH} = 15.0 V, V_{AL} = 0 V	10,11			500	
		See figure 3. M,D,P,L,R 2/	9			500	
Switch turn “OFF” time	tOFF	R_L = 300 Ω, V_S = +3 V	9	01,03		250	ns
		V_{AH} = 4.0 V, V_{AL} = 0 V	10,11			450	
		See figure 3. M,D,P,L,R 2/	9			450	
		R_L = 300 Ω, V_S = +3 V	9	02		250	
		V_{AH} = 15.0 V, V_{AL} = 0 V	10,11			450	
		See figure 3. M,D,P,L,R 2/	9			450	

1/ V- = -15 V and V+ = +15 V. For device types 01 and 03, V_{AH} = +4 V and V_{AL} = 0.8 V and for device type 02, V_{AH} = +11 V and V_{AL} = 3.5 V.

2/ Devices supplied to this drawing will meet all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the R level (see 1.5 herein). Pre and post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for all RHA levels, T_A = +25°C.

3/ Tested initially and after any design changes which may affect these parameters.

4/ For device types 01 and 03, V_{AL} = 0 V and V_{AH} = 4.0 V and for device type 02, V_{AL} = 0 V and V_{AH} = 15 V.

Case outlines	C and X	E and Y
Device types	01 and 02	03
Terminal number	Terminal symbol	
1	NC	D1
2	S3	NC
3	D3	D3
4	D1	S3
5	S1	S4
6	IN1	D4
7	GND	NC
8	V-	D2
9	IN2	S2
10	S2	IN2
11	D2	V+
12	D4	NC
13	S4	GND
14	V+	V-
15	---	IN1
16	---	S1

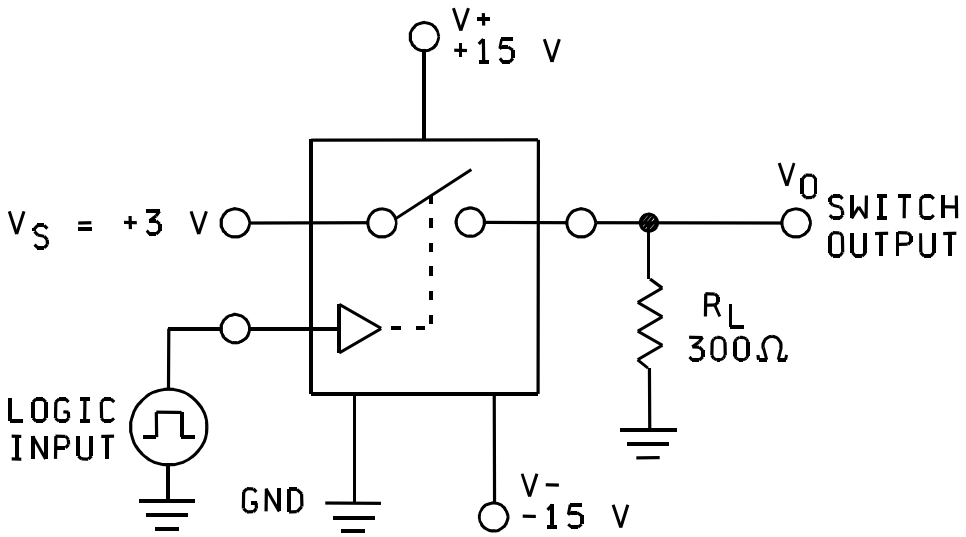
NC = No connections

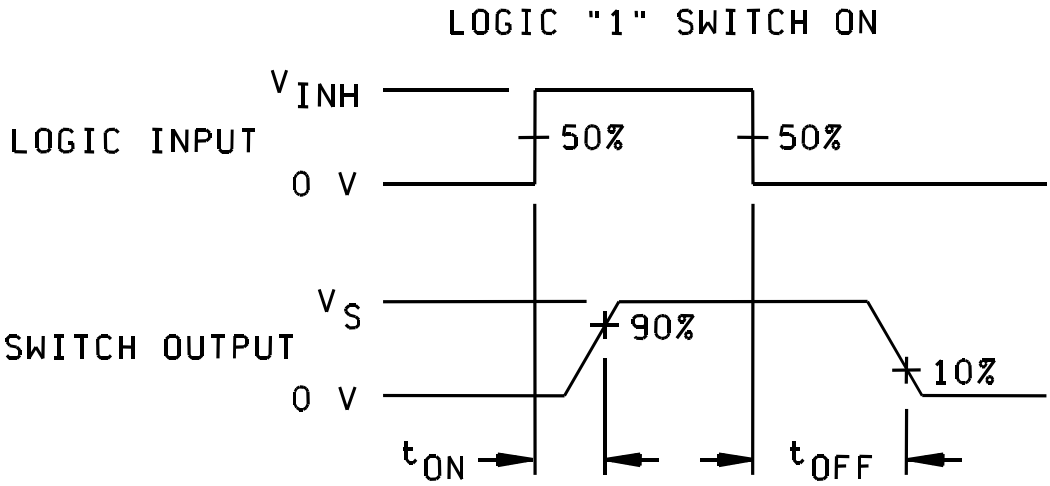
FIGURE 1. Terminal connections.

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

FIGURE 2. Truth table.

SWITCHING TEST CIRCUIT

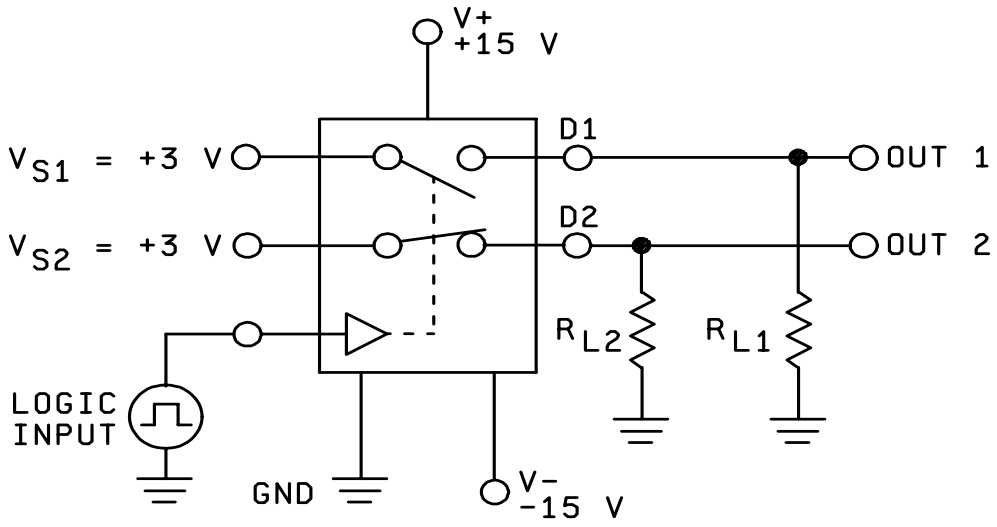


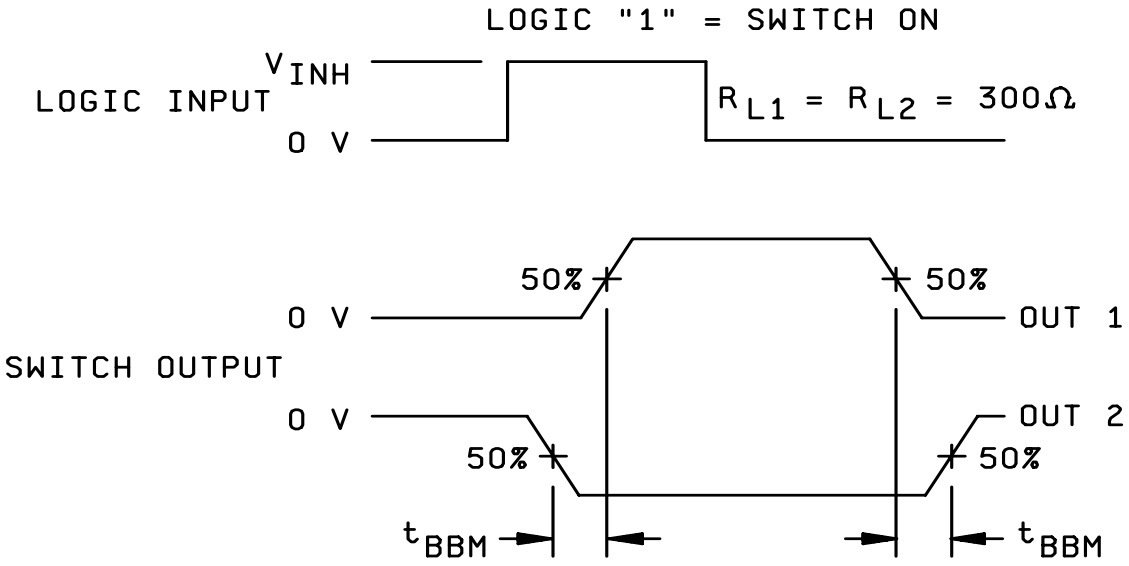


NOTE: For device types 01 and 03, V_{INH} = +4 V. For device type 02, V_{INH} = +15 V.

FIGURE 3. Timing diagram.

BREAK-BEFORE-MAKE TEST CIRCUIT





NOTE: For device types 01 and 03, V_{INH} = +5 V. For device type 02, V_{INH} = +15 V.

FIGURE 3. Timing diagram - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein.

For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's (QM) plan, including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 or as specified in the QM plan including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,9	1,9	1,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,9, 1/ 10,11	1,2,3,9, 1/ 10,11	1,2,3, 1/ 2/ 9,10,11,Δ	
Group A test requirements (see 4.4)	1,2,3,4,9,10,11 3/	1,2,3,4,9, 3/ 10,11	1,2,3,4, 3/ 9,10,11	
Group C end-point electrical parameters (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9, 2/ 10,11	
Group D end-point electrical parameters (see 4.4)	1,9	1,9	1,9	
Group E end-point electrical parameters (see 4.4)	1,9	1,9	1,9	

1/ PDA applies to subgroup 1. For class V to subgroups 1, 9, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table I).
3/ Subgroup 4, if not tested, shall be guaranteed to the limits specified in table I.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{C1}, C_{C2}, C_{OS}, and C_{IS} measurements) should be measured only for initial qualification and after any process or design changes which may affect input or output capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE IIB. Burn-in delta parameters and group C delta parameters (+25°C).

Parameters	Symbol	Conditions	Device type	Delta limits
Switch on resistance	$+R_{DS}$	V_D = 10 V, I_S = -10 mA S1/S2/S3/S4	All	±5 Ω
	$-R_{DS}$	V_D = -10 V, I_S = 10 mA S1/S2/S3/S4	All	±5 Ω
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +14 V, V_D = -14 V S1/S2/S3/S4	All	±2 nA
	$-I_{S(OFF)}$	V_S = -14 V, V_D = +14 V S1/S2/S3/S4	All	±2 nA
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_S = -14 V, V_D = +14 V S1/S2/S3/S4	All	±2 nA
	$-I_{D(OFF)}$	V_S = +14 V, V_D = -14 V S1/S2/S3/S4	All	±2 nA
Leakage current from an "ON" driver into the switch (drain and source)	$+I_{D(ON)}$	V_S = V_D = +14 V S1/S2/S3/S4	All	±2 nA
	$-I_{D(ON)}$	V_S = V_D = -14 V S1/S2/S3/S4	All	±2 nA
Low level input address current	I_{AL}	All channels V_A = 0.8 V	01,03	±100 nA
		All Channels V_A = 3.5 V	02	±100 nA
High level input address current	I_{AH}	All channels V_A = 4.0 V	01,03	±100 nA
		All channels V_A = 11 V	02	±100 nA
Positive supply current	I+	All channels V_A = 0.8 V	01,03	±1 µA
		V_{A1} = 0 V, V_{A2} = 4.0 V and V_{A1} = 4.0 V, V_{A2} = 0 V	01,03	±0.1 mA
		All channels V_A = 0 V	02	±1 µA
		All channels V_A = 15 V	02	±1 µA
Negative supply current	I-	All channels V_A = 0.8 V	01,03	±1 µA
		V_{A1} = 0 V, V_{A2} = 4.0 V and V_{A1} = 4.0 V, V_{A2} = 0 V	01,03	±1 µA
		All channels V_A = 0 V	02	±1 µA
		All channels V_A = 15 V	02	±1 µA

TABLE III. Irradiation test connections - Device types 01 and 03.

Test	Open	Ground	V_1	V_2	V_3
Radiation exposure	1	2,3,4,5,7, 1/ 10,11,12,13	14	8	6,9

1/ Except for pin 7, all pins to GND have a series resistor (R_S) = 10 kΩ ±5%, ¼ W.
2/ V_1 = +15 V ±10%, V_2 = -15 V ±10%, and V_3 = +5 V ±10%.
3/ Device type 03 is packaged and bonded out to device type 01 configuration.

TABLE III. Irradiation test connections - Device type 02.

Test	Open	Ground	V_1	V_2	V_3
Radiation exposure	1	2,3,4,5,7, 1/ 10,11,12,13	14	8	6,9

1/ Except for pin 7, all pins to GND have a series resistor (R_S) = 10 kΩ ±5%, 1/4 W.
2/ V_1 = +15 V ±10%, V_2 = -15 V ±10%, and V_3 = +12 V ±10%.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the Class T Radiation Requirements of MIL-PRF-38535. The end-point electrical parameters for class T devices shall be as specified in Table I, Group A subgroups, or as modified in the QM plan.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535 (see 1.5 herein).

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Dose rate burnout. When required by the customer, test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

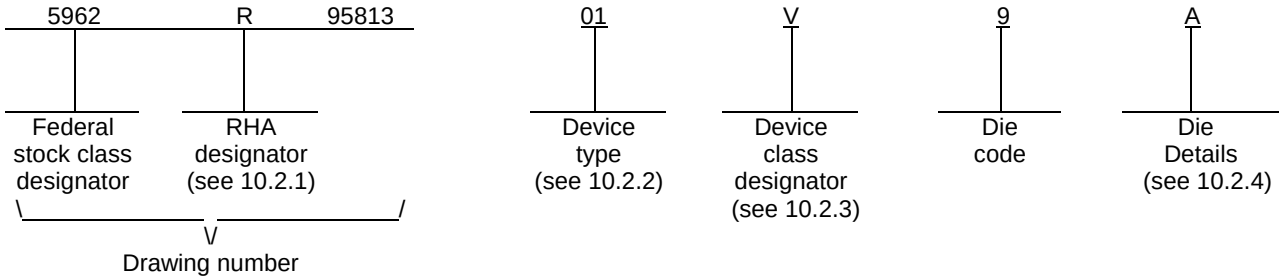
6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A
APPENDIX A IS A PART OF SMD 5962-95813

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-303RH	Radiation hardened DI dual SPST CMOS switch
02	HS-307RH	Radiation hardened DI dual SPST CMOS switch
03	HS-393RH	Radiation hardened DI dual SPST CMOS switch

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2
03	A-3

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-2
03	A-3

10.2.4.3. Interface materials.

Die type	Figure number
01	A-1
02	A-2
03	A-3

10.2.4.4. Assembly related information.

Die type	Figure number
01	A-1
02	A-2
03	A-3

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figures A-1, A-2, and A-3.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figures A-1, A-2, and A-3.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figures A-1, A-2, and A-3.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figures A-1, A-2, and A-3.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3. of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4. of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

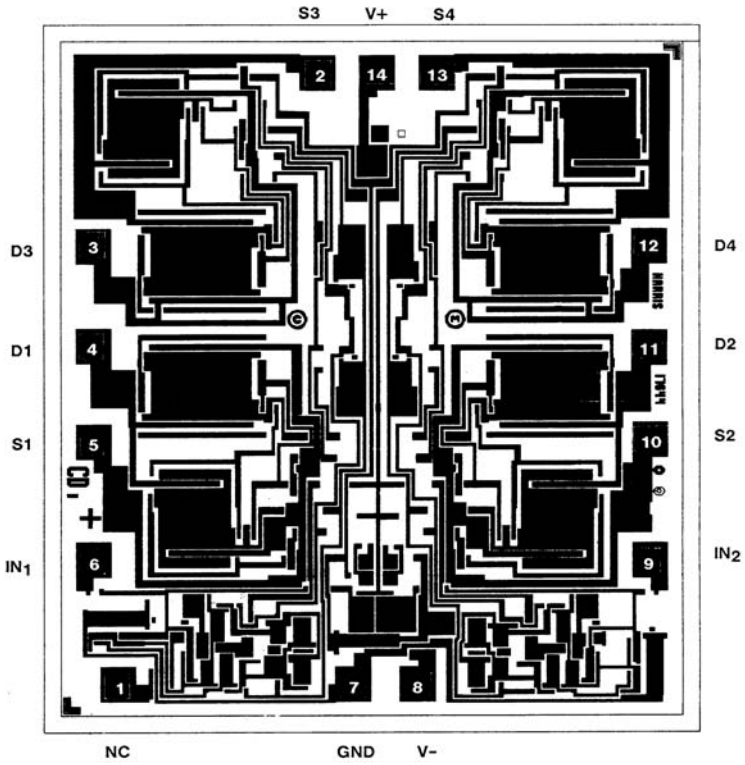
60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A IS A PART OF SMD 5962-95813

Die bonding pad locations and electrical functions

FIGURE A-1 / A-2



NOTE: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

Die physical dimensions.
Die size: 1930 microns x 2130 microns.
Die thickness: 11 ± 1 mils.

Interface materials.
Top metallization: Al 12.5 kÅ ± 2 kÅ
Backside metallization: Gold over polysilicon

Glassivation.
Type: Si02
Thickness: 8 kÅ ± 1 kÅ

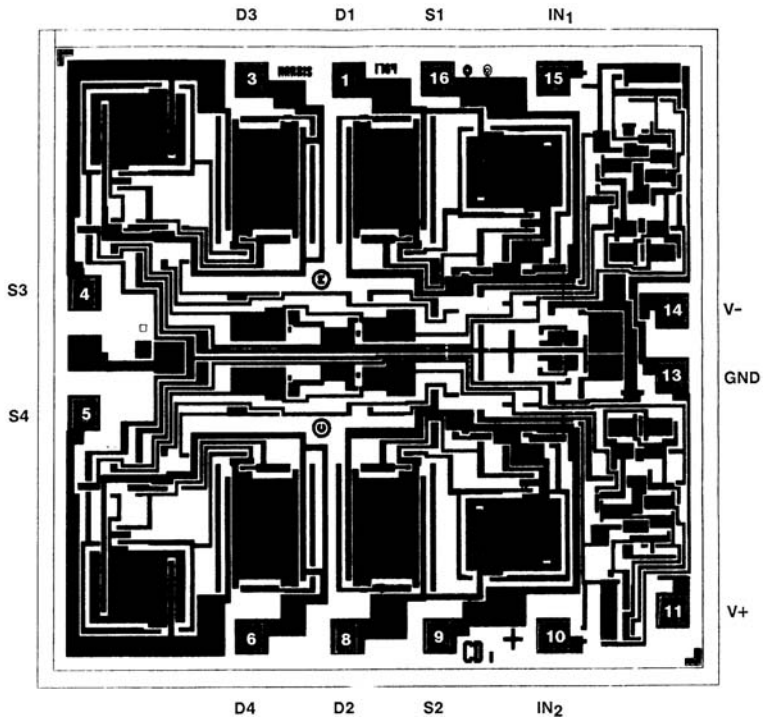
Substrate: DI (dielectric isolation)

Assembly related information.
Substrate potential: Unbiased
Special assembly instructions: None

APPENDIX A
APPENDIX A IS A PART OF SMD 5962-95813

Die bonding pad locations and electrical functions

FIGURE A-3



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E and Y (see figure 1).

Die physical dimensions.
Die size: 2130 microns x 1930 microns.
Die thickness: 11 ± 1 mils.

Interface materials.
Top metallization: Al 12.5 kÅ ± 2 kÅ
Backside metallization: Gold over polysilicon

Glassivation.
Type: Si02
Thickness: 8 kÅ ± 1 kÅ

Substrate: DI (dielectric isolation)

Assembly related information.
Substrate potential: Unbiased
Special assembly instructions: None

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-01-06

Approved sources of supply for SMD 5962-95813 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9581301QCC	34371	HS1-303RH-8
5962R9581301QXC	34371	HS9-303RH-8
5962R9581301TCC	34371	HS1-303RH-T
5962R9581301TXC	34371	HS9-303RH-T
5962R9581301VCC	34371	HS1-303RH-Q
5962R9581301VXC	34371	HS9-303RH-Q
5962R9581301V9A	34371	HS0-303RH-Q
5962R9581302QCC	34371	HS1-307RH-8
5962R9581302QXC	34371	HS9-307RH-8
5962R9581302VCC	34371	HS1-307RH-Q
5962R9581302VXC	34371	HS9-307RH-Q
5962R9581302V9A	34371	HS0-307RH-Q
5962R9581303QEC	34371	HS1-390RH-8
5962R9581303QYC	34371	HS9-390RH-8
5962R9581303TEC	34371	HS1-390RH-T
5962R9581303TYC	34371	HS9-390RH-T

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9581303VEC	34371	HS1-390RH-Q
5962R9581303VYC	34371	HS9-390RH-Q
5962R9581303V9A	34371	HS0-390RH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil 2401 Palm Bay Blvd PO Box 883 Melbourne, FL 32902-0883