M74HC643-1P/FP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643-1 is an integrated circuit chip consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HC643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state inverted and noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

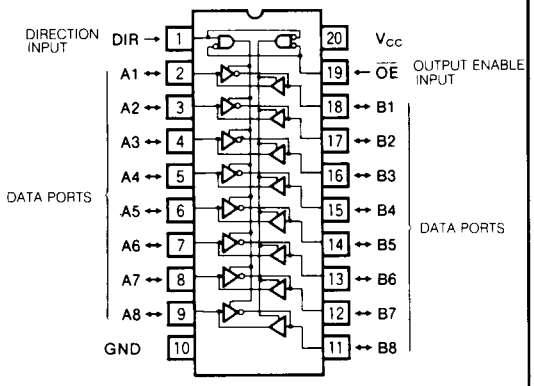
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, the B data ports are set as input terminals and the A data ports are set as output terminals. When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

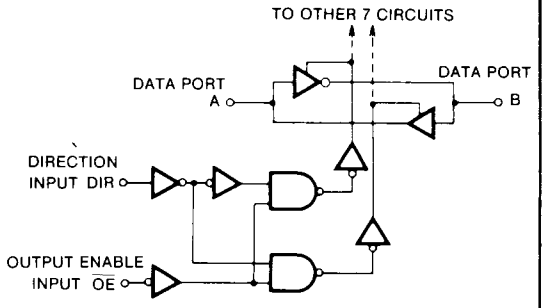
Note 1 : I : Input pin
$\overline{O}$: Output pin (noninverted output)
$\overline{O}$: Output pin (inverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2: M74HC643-1FP: T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40∼+85℃ Min	Limits −40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

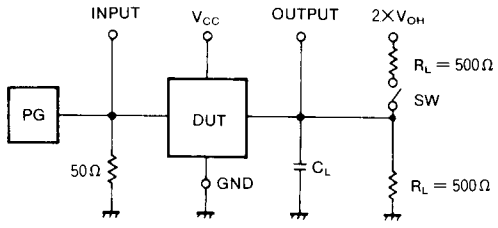
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)				16	ns
t_{PHL}					16	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			27	ns
t_{PZH}					27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)	2.0		17	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{THL}			2.0		24	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−B, B−A)		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PHL}			2.0		25	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PLZ}	Low-level andhigh-level output disable time ($\overline{OE}$ − A, B)		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}			2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		10	24		30	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)		2.0		35	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
t_{PZH}			2.0		36	140		175	ns
			4.5		13	28		35	
			6.0		10	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				53.5				pF

Note 3 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}	Open
t_{PLH}, t_{PHL}	
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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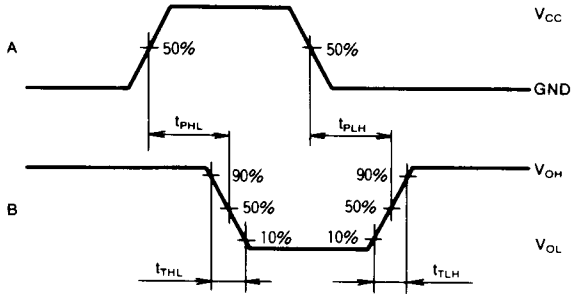
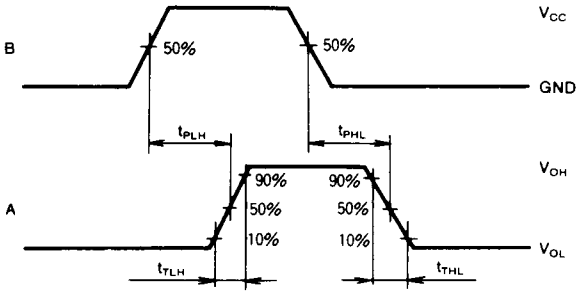
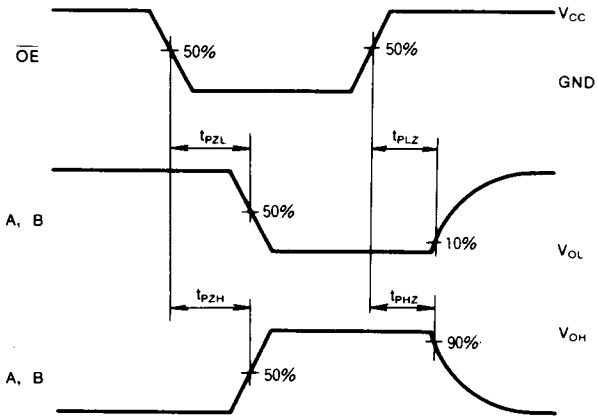
TIMING DIAGRAM





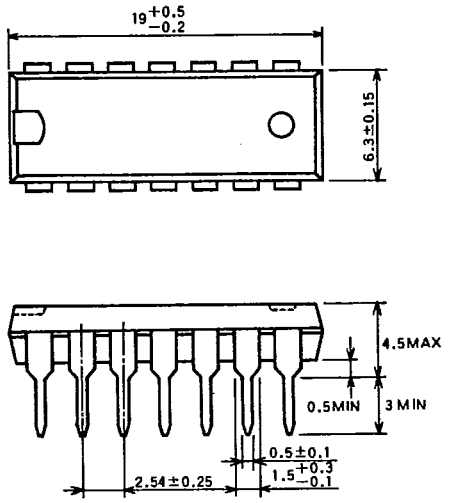


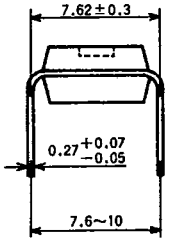
MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

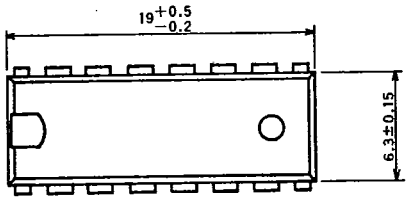
Dimension in mm

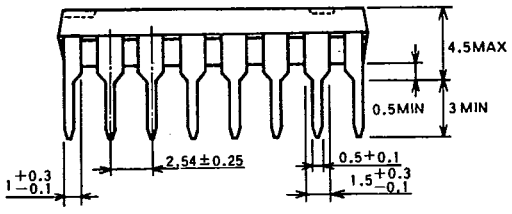


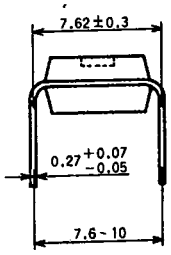


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm





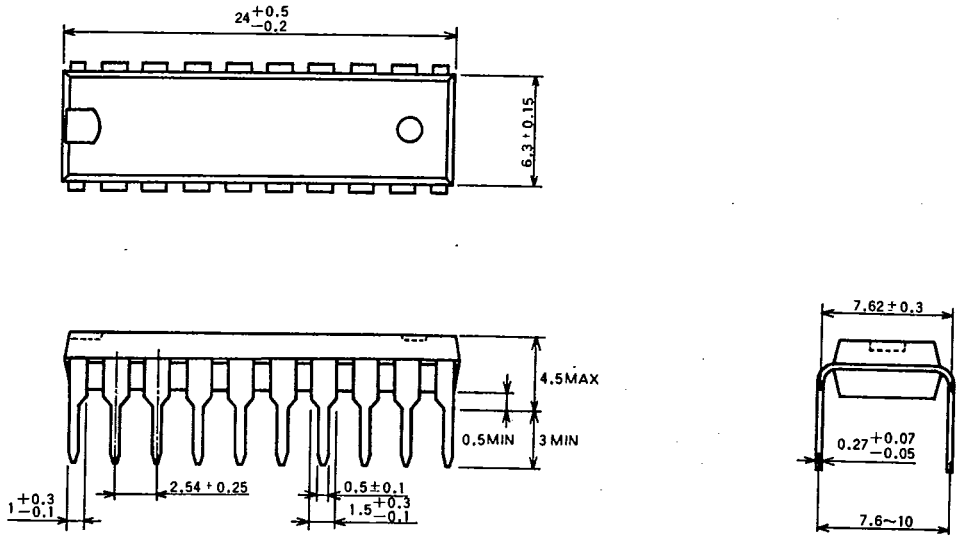


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

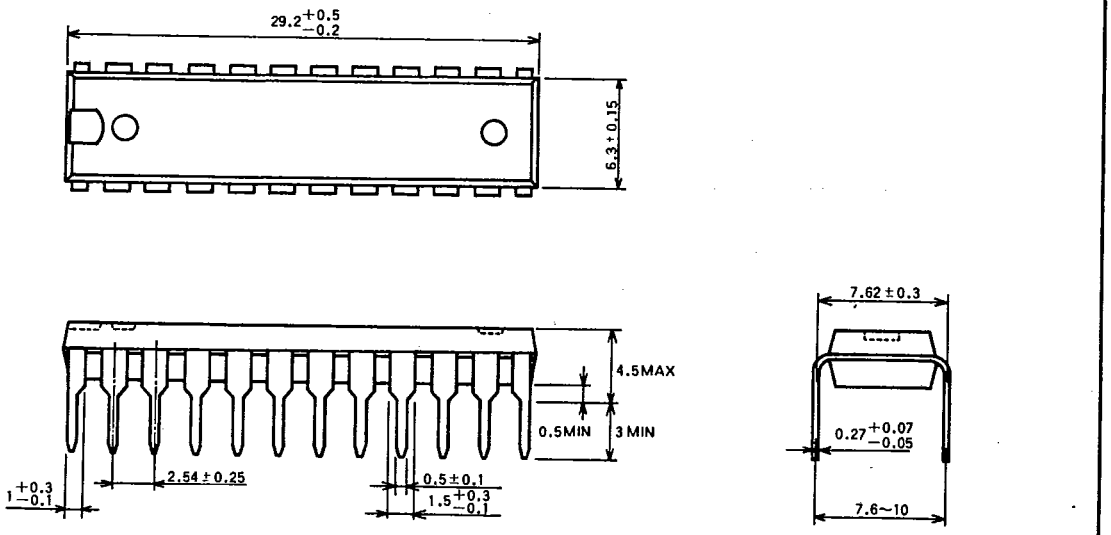
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



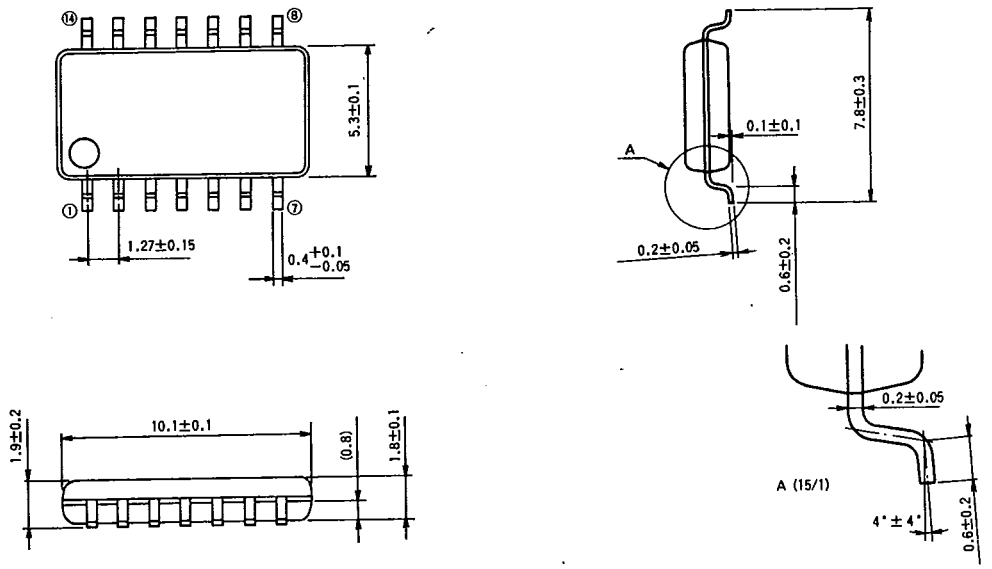
MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

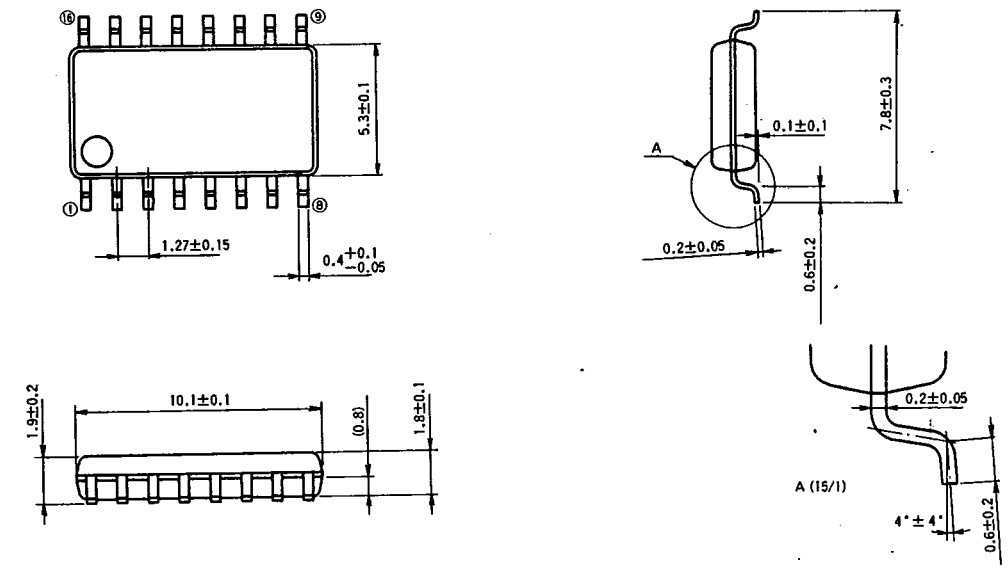
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

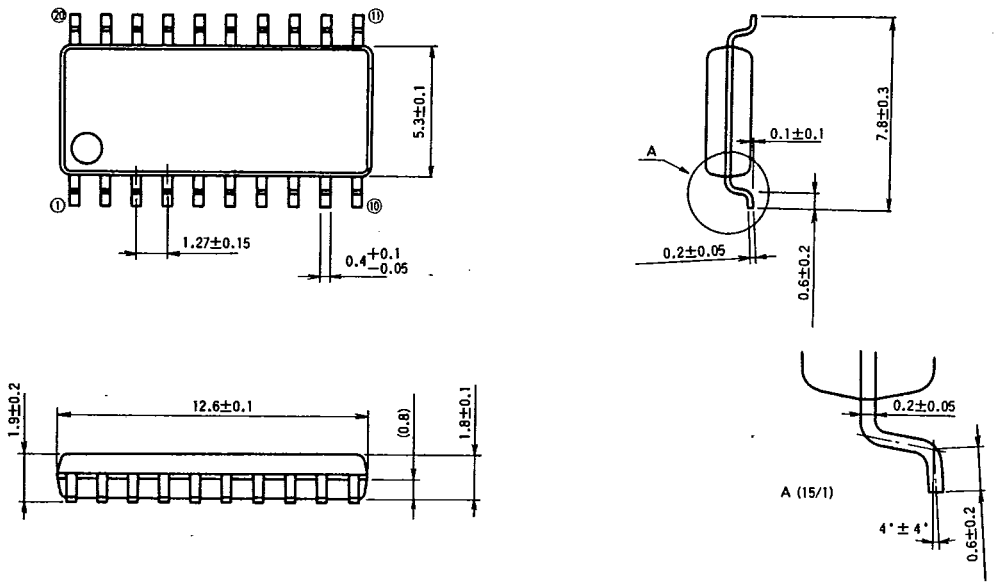
Dimension in mm



PACKAGE OUTLINES

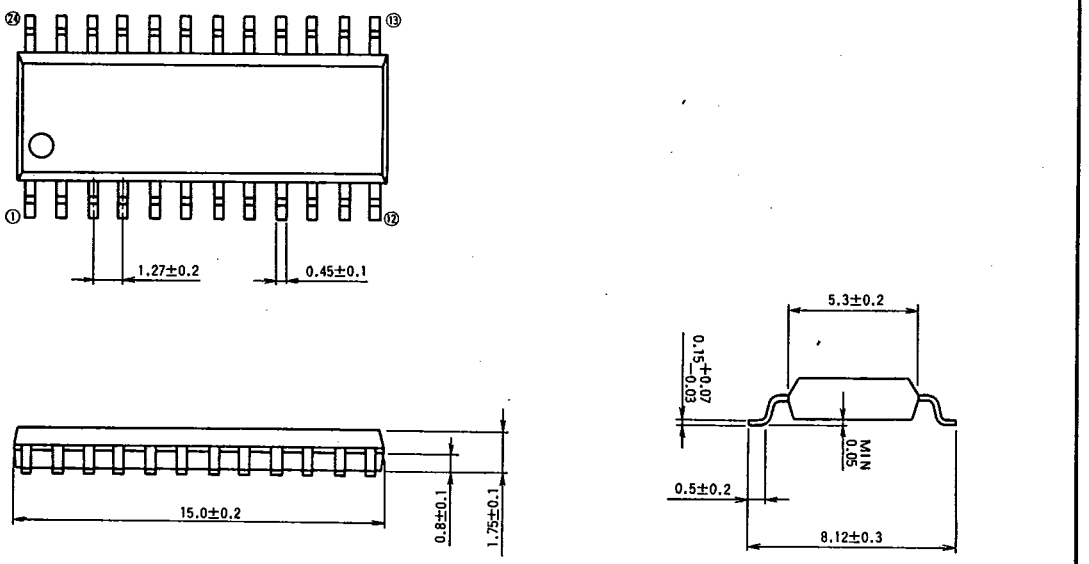
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

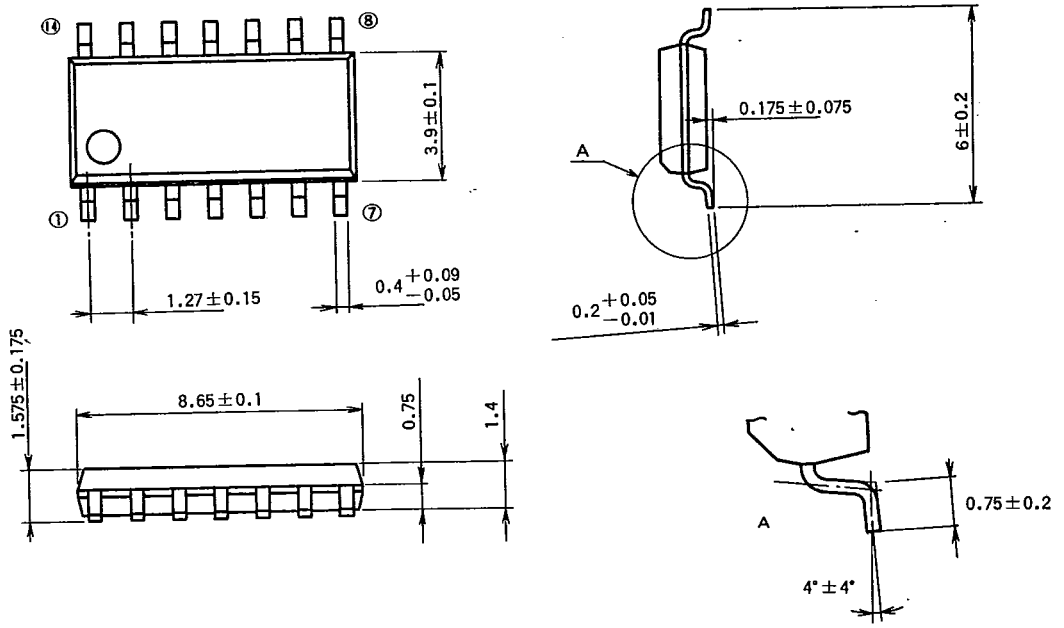


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

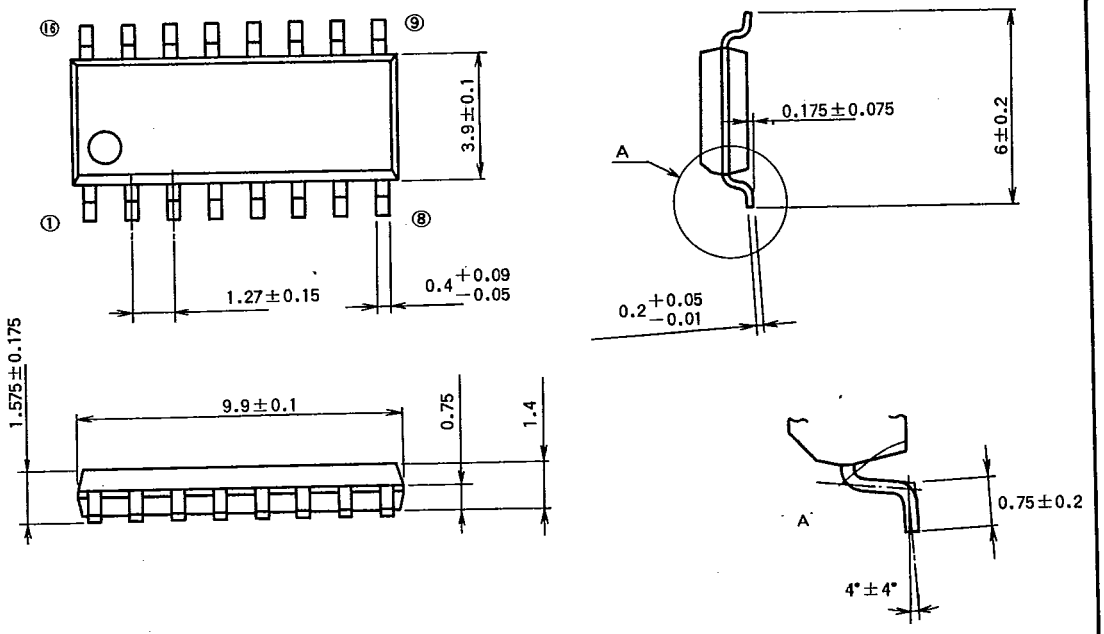
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm