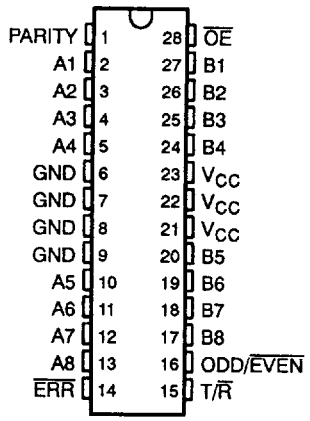
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker and is intended for bus-oriented applications.

The transmit/receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data flows from the A port to the B port (transmit mode); when T/$\overline{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the ODD/$\overline{EVEN}$ input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/$\overline{EVEN}$ input. For example, if ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the $\overline{ERR}$ output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/$\overline{EVEN}$ is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then $\overline{ERR}$ is low, indicating a parity error.

The 74ACT11657 is characterized for operation from −40°C to 85°C.

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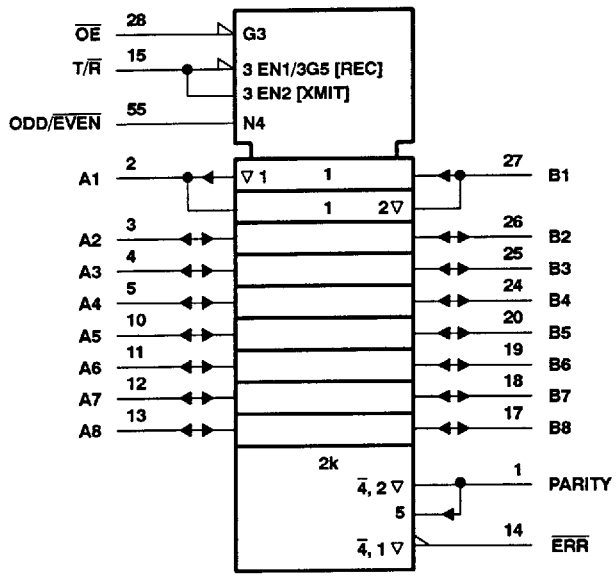
FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

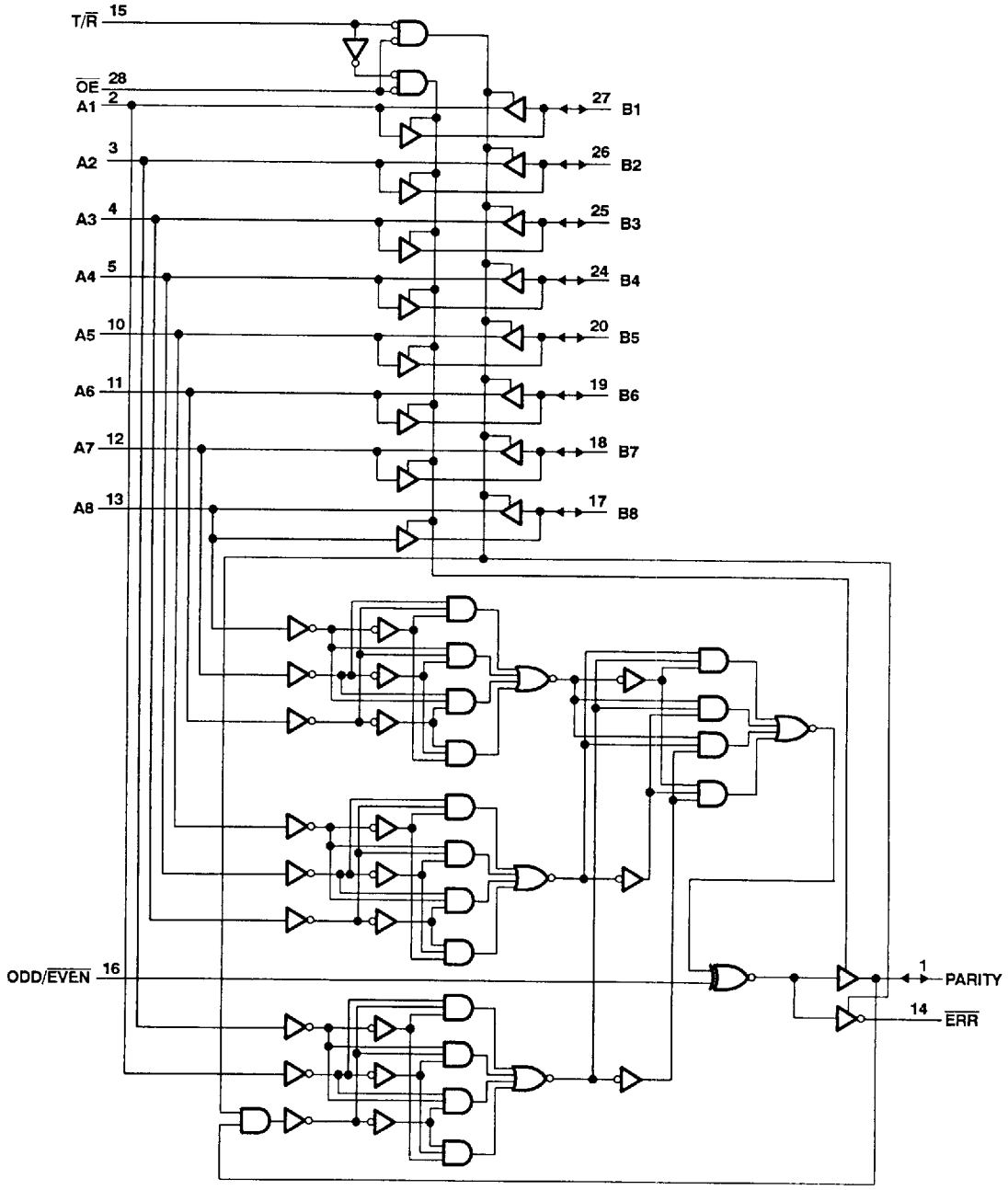


Table 2. Optical Characteristics

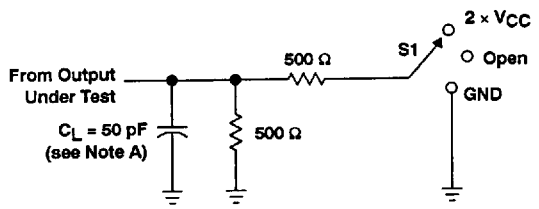
Rated for 1.3 µm wavelength operation. At 10^{-10} BER.

Outline Diagram

operating characteristics, V_{CC} = 5 V, T_A = 25°C

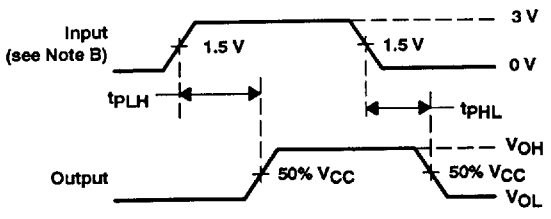
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	95	pF
		Outputs disabled		21	

PARAMETER MEASUREMENT INFORMATION

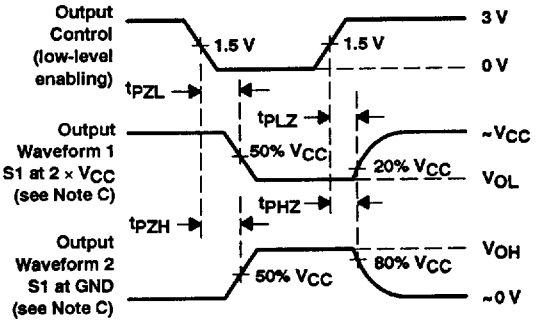


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms