

**8-BIT REGISTERED TRANCEIVERS**
**FEATURES**

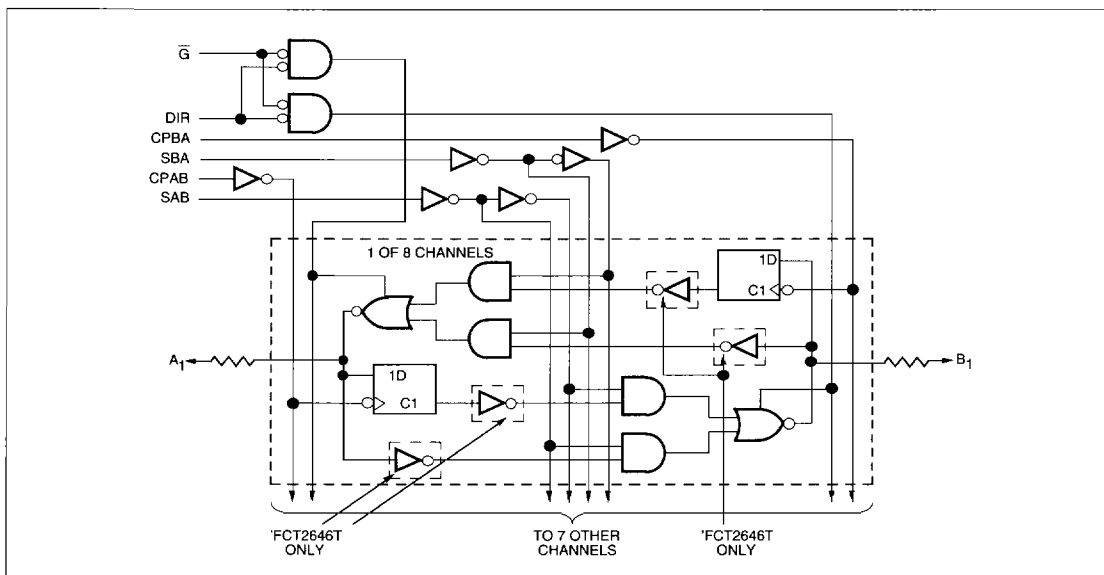
- Function and Pinout Compatible with the FCT and F Logic
- FCT-C speed at 5.4ns max. (Commercial)  
FCT-A speed at 6.3ns max. (Commercial)
- R25Ω output series resistors to reduce transmission line reflection noise
- Reduced V<sub>OH</sub> (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 12 mA Sink Current (Com'l and Mil)  
15 mA Source Current (Com'l and Mil)
- Independent Register for A and B Buses
- 3-State Output

**DESCRIPTION**

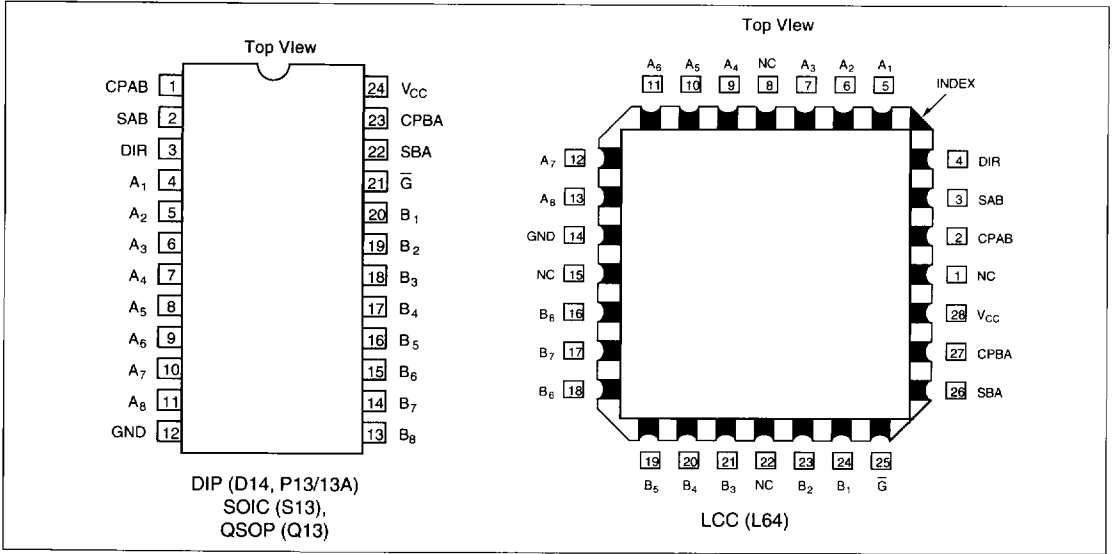
The 'FCT2646T and 'FCT2648T consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control  $\bar{G}$  and direction pins are provided to control the transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the 'FCT2646T and the 'FCT2648 can be used to

replace the 'FCT646T and the 'FCT648, respectively, in an existing design.

In transceiver mode, data present at the high impedance port may be stored in either A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus receives data when enable control  $\bar{G}$  is Active LOW. In isolation mode (enable Control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

**3**
**FUNCTIONAL BLOCK DIAGRAM**


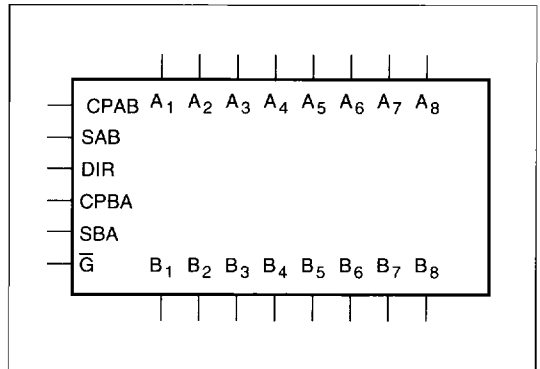
# PIN CONFIGURATIONS

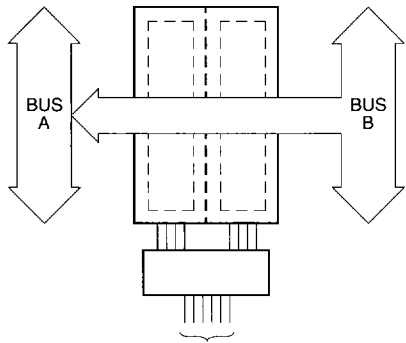


## PIN DESCRIPTION

Pin Names	Description
A <sub>1</sub> - A <sub>8</sub>	Data Register A Inputs Data Register B Outputs
B <sub>1</sub> - B <sub>8</sub>	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\bar{G}$	Output Enable Inputs

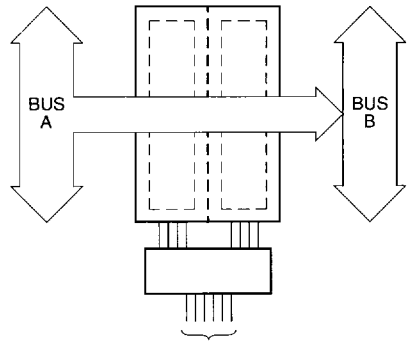
## LOGIC SYMBOL





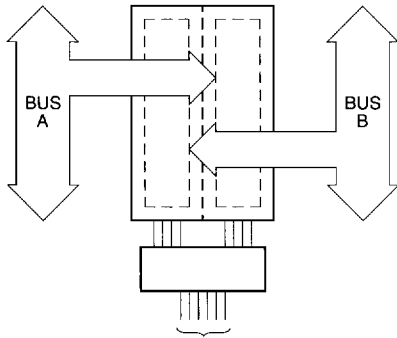
DIR L     $\bar{G}$  L    CPAB X    CPBA X    SAB X    SBA L

**REAL-TIME TRANSFER  
BUS B TO BUS A**



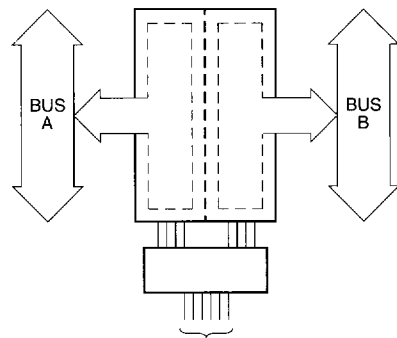
DIR H     $\bar{G}$  L    CPAB X    CPBA X    SAB L    SBA X

**REAL-TIME TRANSFER  
BUS A TO BUS B**



DIR H L X     $\bar{G}$  L L H    CPAB X X    CPBA X X    SAB X X X    SBA X X X

**STORAGE FROM  
A AND/OR B**



DIR<sup>(1)</sup> L H     $\bar{G}$  L L    CPAB X H or L    CPBA X H or L    SAB X H    SBA H X

**TRANSFER STORED  
DATA TO A AND/OR B**

**Note:** Cannot transfer data to A bus and B bus simultaneously.

## FUNCTION TABLE

Inputs						Data I/O <sup>1</sup>		Operation or Function	
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>1</sub> thru A <sub>8</sub>	B <sub>1</sub> thru B <sub>8</sub>	'FCT2646T	'FCT2648T
H	X	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
H	X	┐	┐	X	X				
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\bar{B}$ Data to A Bus Stored B Data to A Bus
L	L	X	H or L	X	H				
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\bar{A}$ Data to B Bus Stored $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X				

**Notes:**

1. The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  or DIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs

2. H = HIGH, L = LOW, X = Don't Care, ┐ = LOW-to-HIGH Transition

## ABSOLUTE MAXIMUM RATINGS<sup>3,4</sup>

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Ambient Temperature Under Bias	-65 to +135	°C
$V_{CC}$	$V_{CC}$ Potential to Ground	-0.5 to +7.0	V
$P_T$	Power Dissipation	0.5	W
$I_{OUTPUT}$	Current Applied to Output	120	mA
$V_{IN}$	Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	Voltage Applied to Output	-0.5 to +7.0	V

## RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage ( $V_{CC}$ )	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ <sup>5</sup>	Max	Units	$V_{CC}$	Conditions
$V_{IH}$	Input HIGH Voltage		2.0			V		
$V_{IL}$	Input LOW Voltage				0.8	V		
$V_H$	Hysteresis <sup>3</sup>			0.2		V		All inputs
$V_{IK}$	Input Clamp Diode Voltage			-0.7	-1.2	V	MIN	$I_{IN} = -18mA$
$V_{OH}$	Output HIGH Voltage	Military	2.4	3.3		V	MIN	$I_{OH} = -12mA$
		Commercial	2.4	3.3		V	MIN	$I_{OH} = -15mA$
$V_{OL}$	Output LOW Voltage	Military		0.3	0.55	V	MIN	$I_{OL} = 12mA$
		Commercial		0.3	0.55	V	MIN	$I_{OL} = 12mA$
$R_{OUT}$	Output Resistance	Military		25		$\Omega$	MIN	$I_{OL} = 12mA$
		Commercial	20	25	40	$\Omega$	MIN	$I_{OL} = 12mA$
$I_I$	Input HIGH Current				20	$\mu A$	MAX	$V_{IN} = V_{CC}$
$I_{IH}$	Input HIGH Current (Except I/O Pins)				5	$\mu A$	MAX	$V_{IN} = 2.7V$
$I_{IL}$	Input LOW Current (Except I/O Pins)				-5	$\mu A$	MAX	$V_{IN} = 0.5V$
$I_{IH}$	Input HIGH Current (I/O Pins only)				15	$\mu A$	MAX	$V_{OUT} = 2.7V$
$I_{IL}$	Input LOW Current (I/O Pins only)				-15	$\mu A$	MAX	$V_{OUT} = 0.5V$
$I_{OS}$	Output Short Circuit Current <sup>6</sup>		-60	-120	-225	mA	MAX	$V_{OUT} = 0.0V$
$I_{OFF}$	Power-off Disable				100	$\mu A$	0V	$V_{OUT} = 4.5V$
$C_{IN}$	Input Capacitance <sup>7</sup>			6	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance <sup>7</sup>			8	12	pF	MAX	All outputs
$I_{CC}$	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$

### Notes:

- Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground.
- Typical values are at  $V_{CC} = 5.0V$ ,  $T_A = +25^\circ C$  ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test

apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

- This parameter is guaranteed but not tested.

## DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ <sup>1</sup>	Max	Units	Conditions
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 3.4V^8$ , $f_1 = 0$ , Outputs Open
$I_{CCD}$	Dynamic Power Supply Current <sup>9</sup>	0.15	0.25	mA/ MHz	$V_{CC} = \text{MAX}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G} = \text{DIR} = \text{GND}$ , or $\text{GAB} = \overline{\text{GBA}} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
$I_C$	Total Power Supply Current <sup>11</sup>	1.7	4.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , $\overline{G} = \text{DIR} = \text{GND}$ , or $\text{GAB} = \overline{\text{GBA}} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , $\overline{G} = \text{DIR} = \text{GND}$ , or $\text{GAB} = \overline{\text{GBA}} = \text{GND}$ , $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		7.0	12.8 <sup>10</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 5\text{MHz}$ , $\overline{G} = \text{DIR} = \text{GND}$ , or $\text{GAB} = \overline{\text{GBA}} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8 <sup>10</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 5\text{MHz}$ , $\overline{G} = \text{DIR} = \text{GND}$ , or $\text{GAB} = \overline{\text{GBA}} = \text{GND}$ , $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

### Notes:

- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_I + I_{CCD} (f_0/2 + f_1 N_I)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

- $D_H$  = Duty Cycle for TTL Inputs High  
 $N_I$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_0$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_1$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.

## AC CHARACTERISTICS

Symbol	Parameter	'FCT2646T/2648T				'FCT2646AT/2648AT				'FCT2646CT/2648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay <sup>13</sup> Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
$t_{PZH}$ $t_{PZL}$	Output Enable Time Enable to Bus and DIR to A or B	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time G to Bus and DIR to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

## AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT2646T/2648T				'FCT2646AT/2648AT				'FCT2646CT/2648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.	Min. <sup>12</sup>	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	5

### Note:

12. Minimum limits are guaranteed but not tested on Propagation Delays.

13. AC Characteristics guaranteed with  $C_L = 50\text{pF}$  as shown in Figure 1.

\*Refer to the 'Parameter Measurement Information' section of this book.

## ORDERING INFORMATION

$\frac{CYxxFCT}{\text{Temp. Class}}$      $\frac{xxxx}{\text{Device type}}$      $\frac{x}{\text{Package}}$      $\frac{x}{\text{Processing}}$

