National Semiconductor

MICROCIRCUIT DATA SHEET

MJCD4001B-X REV 1A0

Original Creation Date: 10/16/95
Last Update Date: 07/30/99
Last Major Revision Date: 06/16/99

QUAD 2-INPUT NOR GATE WITH BUFFERED OUTPUTS

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to Vdd and Vss.

Industry Part Number

CD4001B

NS Part Numbers

JM4001BBCA

Prime Die

CD4001B

Controlling Document

38510/05252, amend. #3

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)
(Note 1, 2)

Voltage at Any Pin	-0.5V to Vdd +0.5V
Power Dissipation (Pd)	200mW
Vdd Range	-0.5V to +18V
Storage Temperature (Ts)	-65C to +150C
Lead Temperature (Tl) (Soldering, 10 seconds)	300C
Input Current (each input)	± 10mA
Maximum Junction Temperature (Tj)	175C
Thermal Resistance, Junction to Case	See MIL-STD-1835

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: All voltages measured with respect to Vss unless otherwise specified.

Recommended Operating Conditions

Operating Range (VDD)	4.5V to 15.0V
Operating Temperature Range	-55C to +125C
Input Low Voltage Range (VIL)	
VDD=5.0V	0V to 1.5V
VDD=10.0V	0V to 2.0V
VDD=15.0V	0V to 4.0V
Input High Voltage Range (VIH)	
VDD=5.0V	3.5V to 5.0V
VDD=10.0V	8.0V to 10.0V
VDD=15.0V	11.0V to 15.0V

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vic+	Input Clamping Voltage (positive)	VDD=0.0V, IIN=1mA	5, 6	INPUTS		1.5	V	1
Vic-	Input Clamping Voltage (negative)	VDD=Open, IIN= -1mA	5, 6	INPUTS		-6.0	V	1
IIH	Input High Current	VDD=18.0V, VM=18.0V, each input measured separately, other inputs at 0.0V	3, 4	INPUTS		100.0	nA	1, 2
IIL	Input Low Current	VDD=18.0V, VM=0.0V, each input measured separately, other inputs at 0.0V	3, 4	INPUTS		-100.0	nA	1, 2
ISS	Power Supply Current	VDD=18.0V, VINH=18.0V, VM=0.0V, one input per gate at VINH, other inputs at 0.0V	3, 4	VSS		-25.0	nA	1
			3, 4	VSS		-750.0	nA	2
		VDD=18.0V, VINL=0.0V, VM=0.0V, all inputs at VINL	3, 4	VSS		-25.0	nA	1
			3, 4	VSS		-750.0	nA	2
VOH	Output High Voltage	VDD=15.0V, VINL=0.0V, IOH=0.0mA, all inputs at VINL	1, 2	OUTPUTS	14.95		V	1, 2, 3
VOL	Output Low Voltage	VDD=15.0V, VINL=0.0V, VINH=15.0V, IOL=0.0mA, one input per gate at VINH, other inputs at VINL	1, 2	OUTPUTS		0.05	V	1, 2, 3
VIH	Input High Voltage	VDD=5.0V, VIL=1.5V, VOUT=0.5V, IOUT=0.0mA	1, 2, 9	INPUTS		3.5	V	1, 2, 3
		VDD=10.0V, VIL=3.0V, VOUT=1.0V, IOUT=0.0mA	1, 2, 9	INPUTS		7.0	V	1, 2, 3
		VDD=15.0V, VIL=4.0V, VOUT=1.5V, IOUT=0.0mA	1, 2, 9	INPUTS		11.0	V	1, 2, 3
VIL	Input Low Voltage	VDD=5.0V, VOUT=4.5V, IOUT=0.0mA	1, 2, 9	INPUTS	1.5		V	1, 2, 3
		VDD=10.0V, VOUT=9.0V, IOUT=0.0mA	1, 2, 9	INPUTS	3.0		V	1, 2, 3
		VDD=15.0V, VOUT=13.5V, IOUT=0.0mA	1, 2, 9	INPUTS	4.0		V	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IOL	Output Low Current	VDD=5.0V, VINH=5.0V, VINL=0.0V, VOL=0.4V	1, 2, 9	OUTPUTS	0.51		mA	1
			1, 2, 9	OUTPUTS	0.36		mA	2
			1, 2, 9	OUTPUTS	0.64		mA	3
		VDD=15.0V, VINH=15.0V, VINL=0.0V, VOL=1.5V	1, 2, 9	OUTPUTS	3.4		mA	1
			1, 2, 9	OUTPUTS	2.4		mA	2
			1, 2, 9	OUTPUTS	4.2		mA	3
IOH	Output High Current	VDD=5.0V, VINH=5.0V, VINL=0.0V, VOH=4.6V	1, 2, 9	OUTPUTS	-0.51		mA	1
			1, 2, 9	OUTPUTS	-0.36		mA	2
			1, 2, 9	OUTPUTS	-0.64		mA	3
		VDD=15.0V, VINH=15.0V, VINL=0.0V, VOH=13.5V	1, 2, 9	OUTPUTS	-3.4		mA	1
			1, 2, 9	OUTPUTS	-2.4		mA	2
			1, 2, 9	OUTPUTS	-4.2		mA	3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD=5.0V, CL=50pF, RL=200K Ohms to ground, Tr/Tf=10 ± 2ns

tpHL	Propagation Delay Time		7, 8	In to On	13	210	nS	9, 11
			7, 8	In to On	18	315	nS	10
tpLH	Propagation Delay Time		7, 8	In to On	13	210	nS	9, 11
			7, 8	In to On	18	315	nS	10
tTHL	Output Transition Time		7, 8	On	10	300	nS	9, 11
			7, 8	On	14	450	nS	10
tTLH	Output Transition Time		7, 8	On	10	410	nS	9, 11
			7, 8	On	14	615	nS	10
Cin	Input Capacitance	VDD=Gnd, f = 1MHz	10	Inputs		12	pF	4

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Delta calculations performed at production burn-in and Group C (operational life test).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ISS	Power Supply Current	VDD=18.0V, VINH=18.0V, VM=0.0V, one input per gate at VINH, other inputs at 0.0V	12	VSS	-10	10	nA	1
		VDD=18.0V, VINL=0.0V, all inputs at VINL	12	VSS	-10	10	nA	1
IOL	Output Low Current	VDD=5.0V, VINH=5.0V, VOL=0.4V	12	OUTPUTS	-15	15	%	1
IOH	Output High Current	VDD=5.0V, VINL=0.0V, VOH=4.6V	12	OUTPUTS	-15	15	%	1

Note 1: Screen tested 100% on each device at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 2: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 3: Screen tested 100% on each device at +25C and +125C temperature only, subgroups A1 and 2.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C and +125C temperature only, subgroups A1 and 2.
Note 5: Screen tested 100% on each device at +25C temperature only, subgroup A1.
Note 6: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup A1.
Note 7: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 8: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A9, 10 and 11.
Note 9: VIL, VIH, IOL and IOH are guaranteed by applying specified conditions and testing VOL and VOH.
Note 10: Guaranteed parameter. This test is only performed during qualification.
Note 11: Guaranteed parameter, not tested.
Note 12: Drift Values need not be calculated if post burn-in electrical test is performed within 24 hours after burn-in.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003456	07/30/99	Donald B. Miller	1) Archive MDS MJCD4001BM-X, rev 0BL and release MDS MJCD4001B-X, rev 1A0. 2) Change IIH limit from 1nA to 100nA. 3) Change IIL limit from -1nA to -100nA.