- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

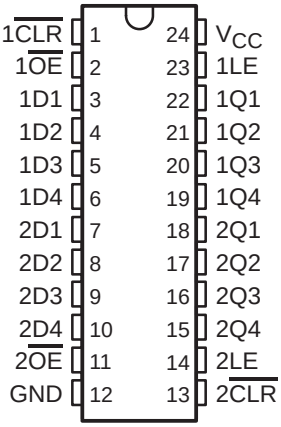
description

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

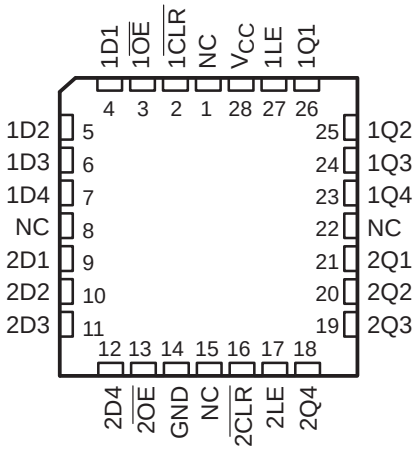
The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear ($\overline{CLR}$) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C.

SN54ALS873B, SN54AS873A . . . JT PACKAGE
SN74ALS873B, SN74AS873A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS873B, SN54AS873A . . . FK PACKAGE
(TOP VIEW)

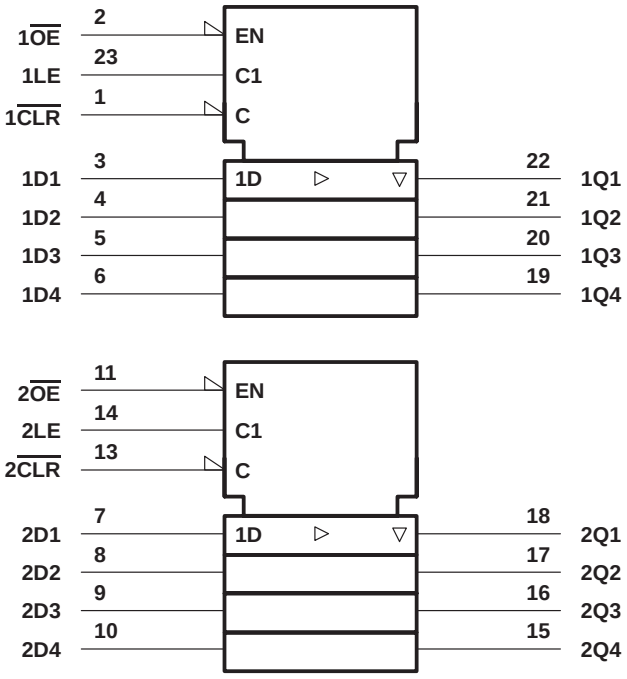


NC – No internal connection

FUNCTION TABLE
(each latch)

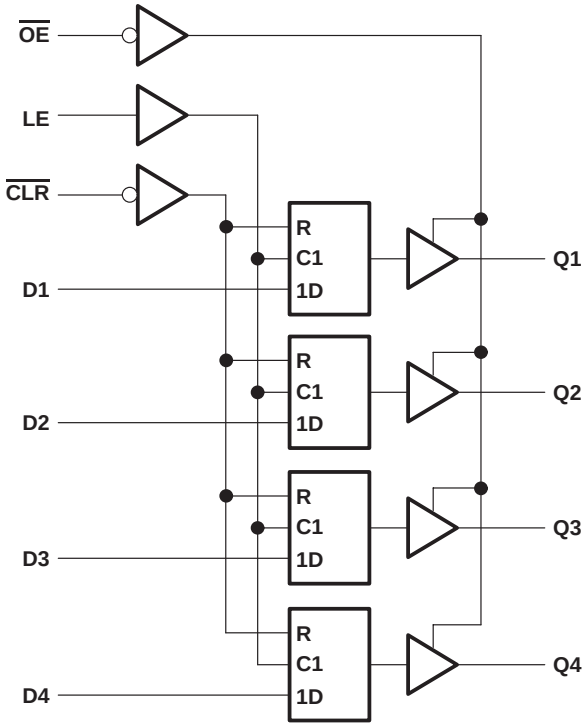
INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	LE	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS873B . . . . . –55°C to 125°C
SN74ALS873B . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS873B			SN74ALS873B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873B			SN74ALS873B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} – 2			V_{CC} – 2			V
	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3					
		I_{OH} = –2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.2			– 0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	21		11	21	mA
		Outputs low		16	29		16	29	
		Outputs disabled		20	31		20	31	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ALS873B		SN74ALS873B		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	15		15		ns
		LE high	10		10		
t_{su}	Setup time, data before LE↓		10		10		ns
t_h	Hold time, data after LE↓		7		7		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS873B		SN74ALS873B		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	23	2	14	ns
t_{PHL}			2	17	2	14	
t_{PLH}	LE	Q	8	31	8	22	ns
t_{PHL}			8	26	8	21	
t_{PHL}	$\overline{CLR}$	Q	6	27	6	20	ns
t_{PZH}	$\overline{OE}$	Q	4	24	4	18	ns
t_{PZL}			4	23	4	18	
t_{PHZ}	$\overline{OE}$	Q	2	12	2	10	ns
t_{PLZ}			2	30	2	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS873A . . . . . –55°C to 125°C
SN74AS873A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS873A			SN74AS873A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873A			SN74AS873A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} – 2			V_{CC} – 2			V
	V_{CC} = 4.5 V	I_{OH} = –12 mA	2.4	3.2					
		I_{OH} = –15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 32 mA		0.25	0.5				V
		I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		68	110		68	110	mA
		Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54AS873A		SN74AS873A		UNIT
			MIN	MAX	MIN	MAX	
t_w*	Pulse duration	$\overline{CLR}$ low	5		5		ns
		LE high	6		5		
t_{su}*	Setup time, data before LE↓		2		2		ns
t_h*	Hold time, data after LE↓		4.5		4.5		ns

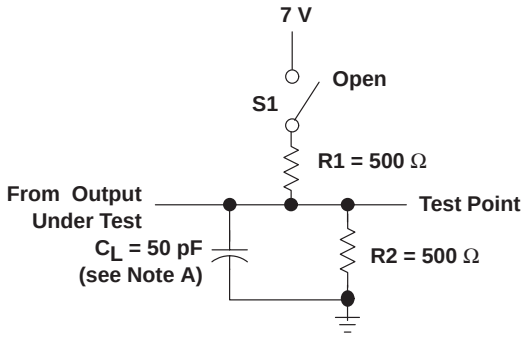
* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54AS873A		SN74AS873A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	12.5	3	9.5	ns
t_{PHL}			3	8.5	3	7.5	
t_{PLH}	LE	Q	6	15.5	6	13	ns
t_{PHL}			4	9	4	7.5	
t_{PHL}	$\overline{CLR}$	Q	3	10.5	3	9	ns
t_{PZH}	$\overline{OE}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	10.5	
t_{PHZ}	$\overline{OE}$	Q	2	8	2	7.5	ns
t_{PLZ}			2	8.5	2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

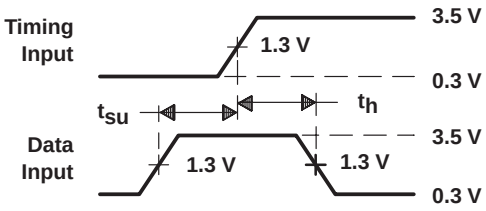
PARAMETER MEASUREMENT INFORMATION



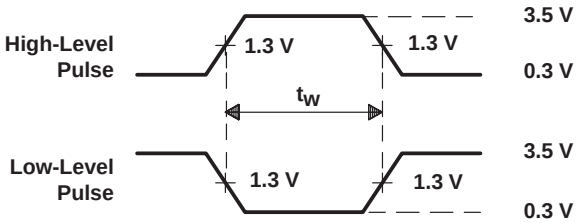
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

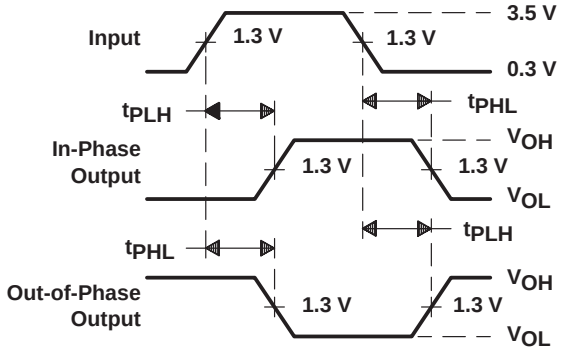
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



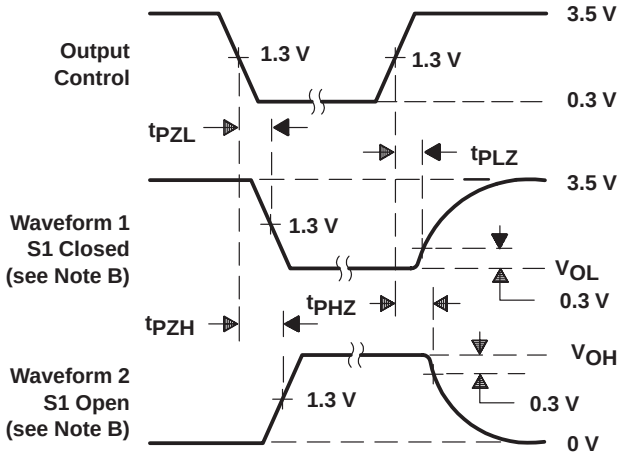
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN54ALS873B, Dual 4-Bit D-type Latches With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS873B	SN74ALS873B
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-2.6/24
No. of Outputs	8	8
Static Current		25
th (ns)		7
tpd max (ns)		14
tsu (ns)		10
Logic	True	True

FEATURES

Back to Top

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

DESCRIPTION

Back to Top

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear ($\overline{CLR}$) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

Product Folder: SN54ALS873B, Dual 4-Bit D-type Latches With 3-State Outputs

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn54als873b.pdf (121 KB,Rev.D) (Updated: 08/01/1995)

APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

Back to Top

- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

Back to Top

- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

Back to Top

DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
84032013A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 16.22	1
8403201KA	OBSOLETE	CFP (W) | 24	-55 TO 125		View Contents	1KU |	
8403201LA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 7.34	1
SN54ALS873BJT	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 6.25	1
SNJ54ALS873BFK	ACTIVE	LCCC (FK) | 28	-55 TO 125	84032013A	View Contents	1KU | 16.22	1

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
6*	3770 | 20 May	8 WKS
	>10k | 27 May	
0*		Call**
299*	>10k | 20 May	8 WKS
0*	>10k | 20 May	8 WKS
0*	3668 | 20 May	8 WKS
	>10k | 27 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
Rochester Electronics | Americas	58	BUY NOW
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		

Product Folder: SN54ALS873B, Dual 4-Bit D-type Latches With 3-State Outputs

SNJ54ALS873BJT	ACTIVE	CDIP (JT)	24	-55 TO 125	8403201LA	View Contents	1KU	7.34	1	185*	>10k	20 May	8 WKS	None Reported View Distributors

Table Data Updated on: 4/17/2003