# DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Bus-Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Choice of True or Inverting Logic**
  - **'ALS878, 'AS878 True Outputs**
  - **'ALS879, 'AS879 Inverting Outputs**
- **Synchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

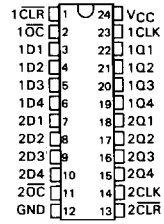
## description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

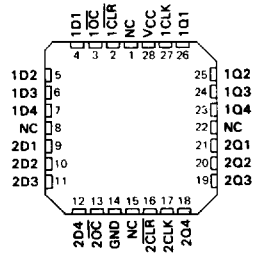
The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS878, SN54ALS879, SN54AS878, and SN54AS879 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS878, SN74ALS879, SN74AS878, and SN74AS879 are characterized for operation from 0°C to 70°C.

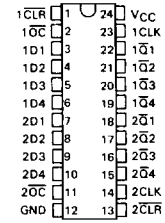
**SN54ALS878, SN54AS878 . . . JT PACKAGE**
**SN74ALS878, SN74AS878 . . . NT PACKAGE**
**(TOP VIEW)**



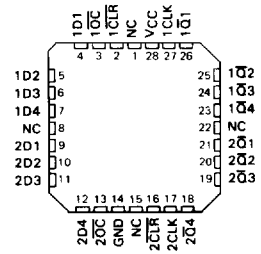

**SN54ALS878, SN54AS878 . . . FH PACKAGE**
**SN74ALS878, SN74AS878 . . . FN PACKAGE**
**(TOP VIEW)**




**SN54ALS879, SN54AS879 . . . JT PACKAGE**
**SN74ALS879, SN74AS879 . . . NT PACKAGE**
**(TOP VIEW)**




**SN54ALS879, SN54AS879 . . . FH PACKAGE**
**SN74ALS879, SN74AS879 . . . FN PACKAGE**
**(TOP VIEW)**




NC—No internal connection

## FUNCTION TABLES

'ALS878, 'AS878
(EACH FLIP-FLOP)

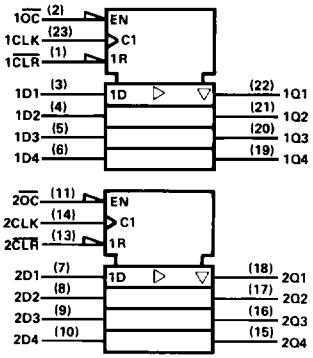
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OC}$ | $\overline{CLR}$ | CLK | D | Q |
| L | L | ↑ | X | L |
| L | H | ↑ | H | H |
| L | H | ↑ | L | L |
| L | H | L | X | $Q_0$ |
| H | X | X | X | Z |

'ALS879, 'AS879
(EACH FLIP-FLOP)

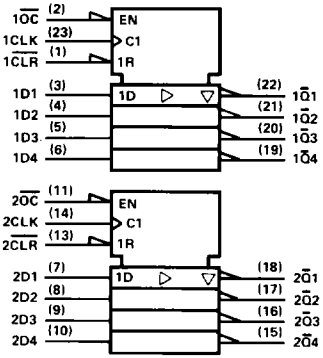
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OC}$ | $\overline{CLR}$ | CLK | D | $\overline{Q}$ |
| L | L | ↑ | X | H |
| L | H | ↑ | H | L |
| L | H | ↑ | L | H |
| L | H | L | X | $Q_0$ |
| H | X | X | X | Z |

### logic symbols

'ALS878, 'AS878

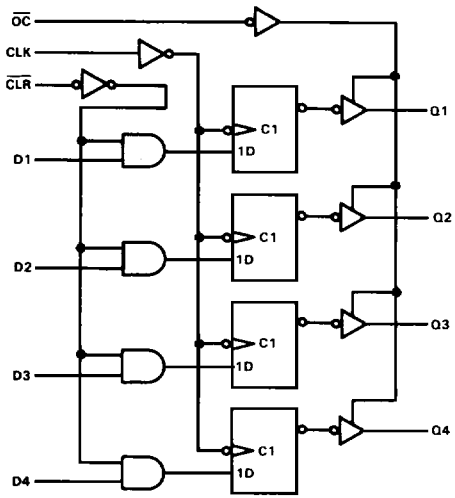



'ALS879, 'AS879

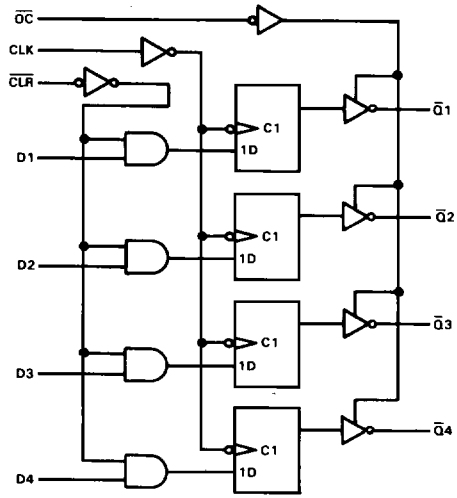



### logic diagrams (positive logic)

'ALS878, 'AS878 (EACH QUAD FLIP-FLOP)




'ALS879, 'AS879 (EACH QUAD FLIP-FLOP)




Pin numbers shown are for JT and NT packages.



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS878, SN54ALS879 . . . . . −55°C to 125°C
SN74ALS878, SN74ALS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

**recommended operating conditions**

| | | | SN54ALS878 SN54ALS879 | | | SN74ALS878 SN74ALS879 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −1 | | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | | | | 12 | | | 24 | mA |
| $f_{clock}$ | Clock frequency | 'ALS878 | 0 | | 25 | 0 | | 30 | MHz |
| | | 'ALS879 | 0 | | 20 | 0 | | 25 | |
| $t_w$ | Pulse duration | 'ALS878 CLK high or low | 20 | | | 16.5 | | | ns |
| | | 'ALS879 CLK high or low | 25 | | | 20 | | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 15 | | | 15 | | | ns |
| | | $\overline{CLR}$ | 20 | | | 20 | | | |
| $t_h$ | Hold time after CLK↑ | Data | 4 | | | 4 | | | ns |
| | | $\overline{CLR}$ | 0 | | | 0 | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | | SN54ALS878 SN54ALS879 | | | SN74ALS878 SN74ALS879 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.4 | 3.3 | | | | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | | | −20 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | | | −0.2 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −15 | | −70 | −15 | | −70 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 14 | 21 | | 14 | 21 | mA |
| | | Outputs low | | 18 | 29 | | 18 | 29 | |
| | | Outputs disabled | | 20 | 31 | | 20 | 31 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

**switching characteristics (see Note 1)**

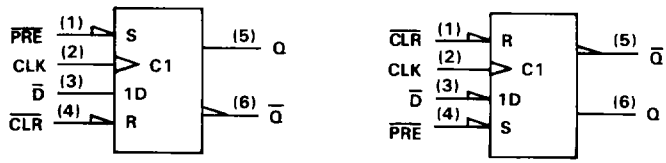
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS878 SN54ALS879 | | SN74ALS878 SN74ALS879 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | 'ALS878 | | 25 | | 30 | | MHz |
| | 'ALS879 | | 20 | | 25 | | |
| $t_{PLH}$ | CLK | Q ('ALS878) or $\overline{Q}$ ('ALS879) | 4 | 15 | 4 | 14 | ns |
| $t_{PHL}$ | | | 4 | 17 | 4 | 16 | |
| $t_{PZH}$ | $\overline{OC}$ | Q ('ALS878) or $\overline{Q}$ ('ALS879) | 4 | 22 | 4 | 20 | ns |
| $t_{PZL}$ | | | 4 | 22 | 4 | 20 | |
| $t_{PHZ}$ | $\overline{OC}$ | Q ('ALS878) or $\overline{Q}$ ('ALS879) | 2 | 12 | 2 | 10 | ns |
| $t_{PLZ}$ | | | 3 | 16 | 3 | 13 | |

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

### D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.




Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.





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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS878, SN54AS879 . . . . . −55°C to 125°C
SN74AS878, SN74AS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

**recommended operating conditions**

| | | | SN54AS878 SN54AS879 | | | SN74AS878 SN74AS879 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | | 32 | | | 48 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 100 | 0 | | 125 | MHz |
| $t_w$ | Pulse duration | CLK low | 3 | | | 2 | | | ns |
| | | CLK high | 5 | | | 4 | | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 3 | | | 2 | | | ns |
| | | $\overline{CLR}$ | 6.5 | | | 5.5 | | | |
| $t_h$ | Hold time after CLK↑ | Data | 3 | | | 2 | | | ns |
| | | $\overline{CLR}$ | 0 | | | 0 | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | SN54AS878 SN54AS879 | | | SN74AS878 SN74AS879 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$ −2 | | | $V_{CC}$ −2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −12 mA | 2.4 | 3.2 | | | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | | | | 2.4 | 3.3 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 32 mA | | 0.29 | 0.5 | | | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | | | 0.33 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | | | −50 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | D | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −3 | | | −2 | mA |
| | All other | | | | | −0.5 | | | −0.5 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | 'AS878 | $V_{CC}$ = 5.5 V, See Note 1 | Outputs high | | 82 | 132 | | 82 | 132 | mA |
| | | | Outputs low | | 96 | 155 | | 96 | 155 | |
| | | | Outputs disabled | | 100 | 160 | | 100 | 160 | |
| | 'AS879 | | Outputs high | | 88 | 142 | | 88 | 142 | |
| | | | Outputs low | | 94 | 150 | | 94 | 150 | |
| | | | Outputs disabled | | 100 | 160 | | 100 | 160 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.
NOTE 1: $I_{CC}$ is measured with CLR and all D inputs grounded, and CLK and OC at 4.5 V.

**switching characteristics (see Note 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS878 SN54AS879 | | SN74AS878 SN74AS879 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | | 125 | | MHz |
| $t_{PLH}$ | CLK | Q ('AS878) or $\overline{Q}$ ('AS879) | 3 | 11.5 | 3 | 8.5 | ns |
| $t_{PHL}$ | | | 4 | 12.5 | 4 | 10.5 | |
| $t_{PZH}$ | $\overline{OC}$ | Q ('AS878) or $\overline{Q}$ ('AS879) | 2 | 8 | 2 | 7 | ns |
| $t_{PZL}$ | | | 3 | 11.5 | 3 | 10.5 | |
| $t_{PHZ}$ | $\overline{OC}$ | Q ('AS878) or $\overline{Q}$ ('AS879) | 2 | 7 | 2 | 6 | ns |
| $t_{PLZ}$ | | | 2 | 7 | 2 | 6 | |

NOTE 1: For load circuit and voltage waveforms, see page 1-12.





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