

54F/74F138

1-of-8 Decoder/Demultiplexer

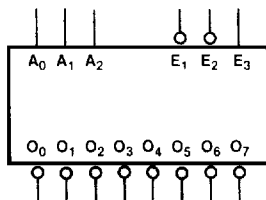
Description

The 'F138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'F138 devices or a 1-of-32 decoder using four 'F138 devices and one inverter.

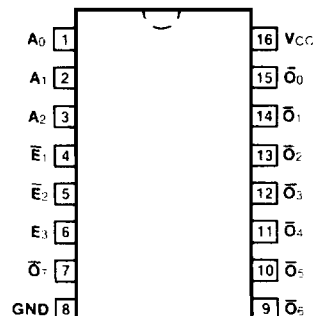
- **FAST Process for High Speed**
- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active LOW Mutually Exclusive Outputs**

Ordering Code: See Section 5

Logic Symbol

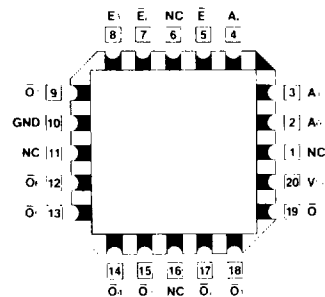


Connection Diagrams



**Pin Assignment
for DIP and SOIC**

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**Pin Assignment
for LCC and PCC**

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A ₀ -A ₂	Address Inputs	0.5/0.375
E ₁ , E ₂	Enable Inputs (Active LOW)	0.5/0.375
E ₃	Enable Input (Active HIGH)	0.5/0.375
O ₀ -O ₇	Outputs (Active LOW)	25/12.5

Functional Description

The 'F138 high-speed 1-of-8 decoder/multiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\bar{O}_0-\bar{O}_7$). The 'F138 features three Enable inputs, two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32

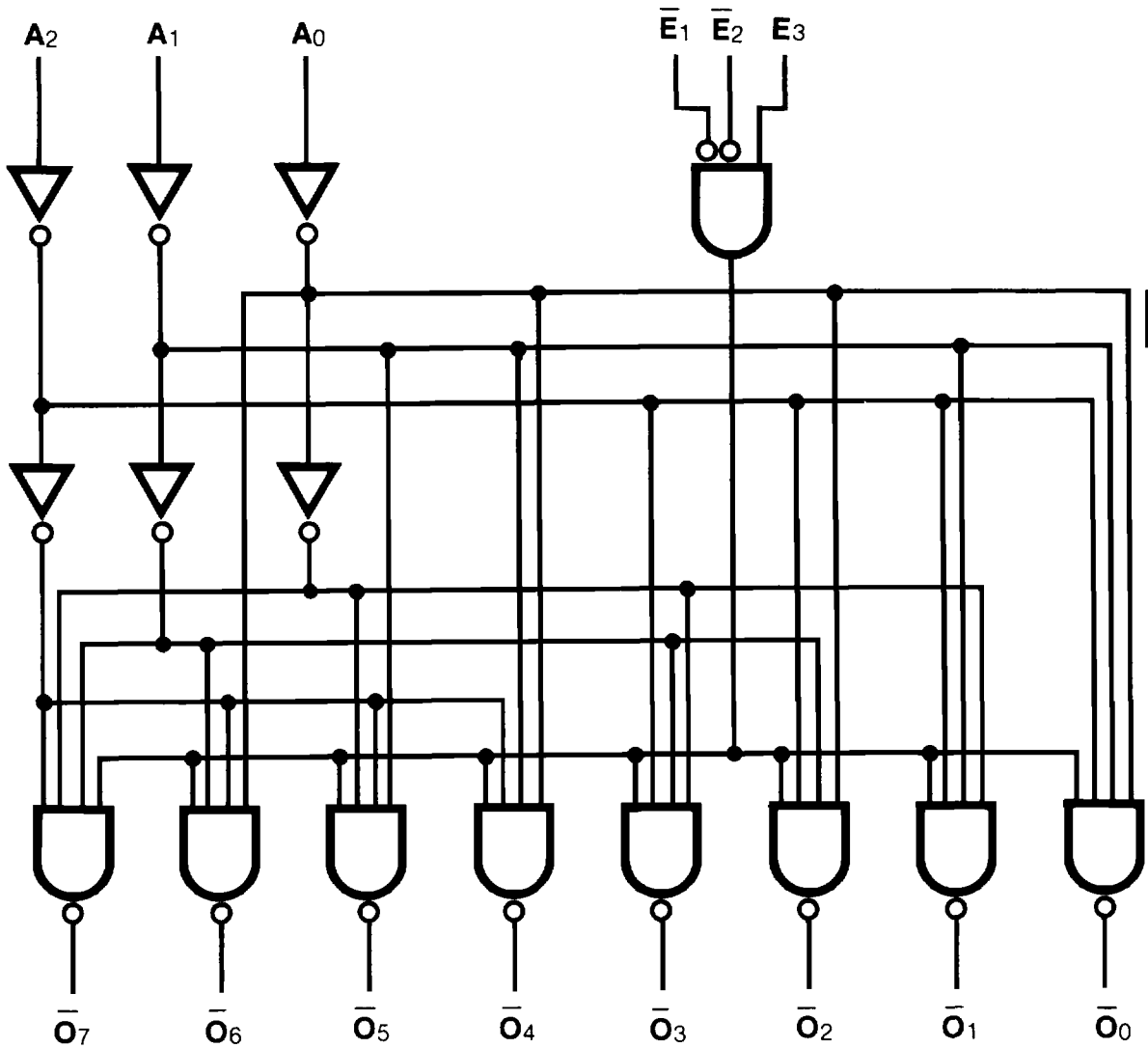
lines) decoder with just four 'F138 devices and one inverter (See Figure a). The 'F138 can be used as an 9-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

Truth Table

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

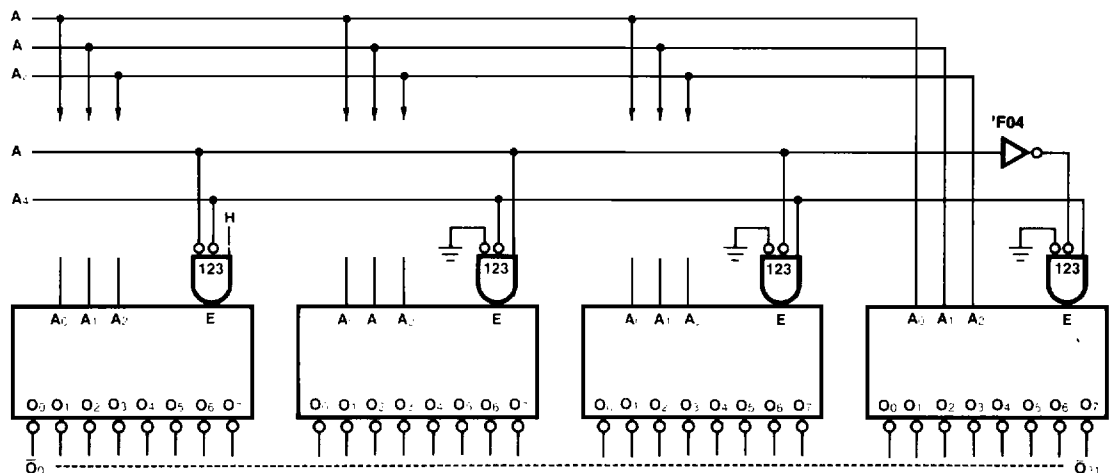
Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fig. a Expansion to 1-of-32 Decoding



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13	20	mA	$V_{CC} = \text{Max}$

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to \bar{O}_n	3.5 4.0	5.6 6.1	7.5 8.0	3.5 4.0	12.0 9.5	3.5 4.0	8.5 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	3.5 3.0	5.4 5.3	7.0 7.0	3.5 3.0	11.0 8.0	3.5 3.0	8.0 7.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_3 to \bar{O}_n	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	12.5 8.5	4.0 3.5	9.0 8.5	ns	3-1 3-3