Q
QUALITY
SEMICONDUCTOR, INC.

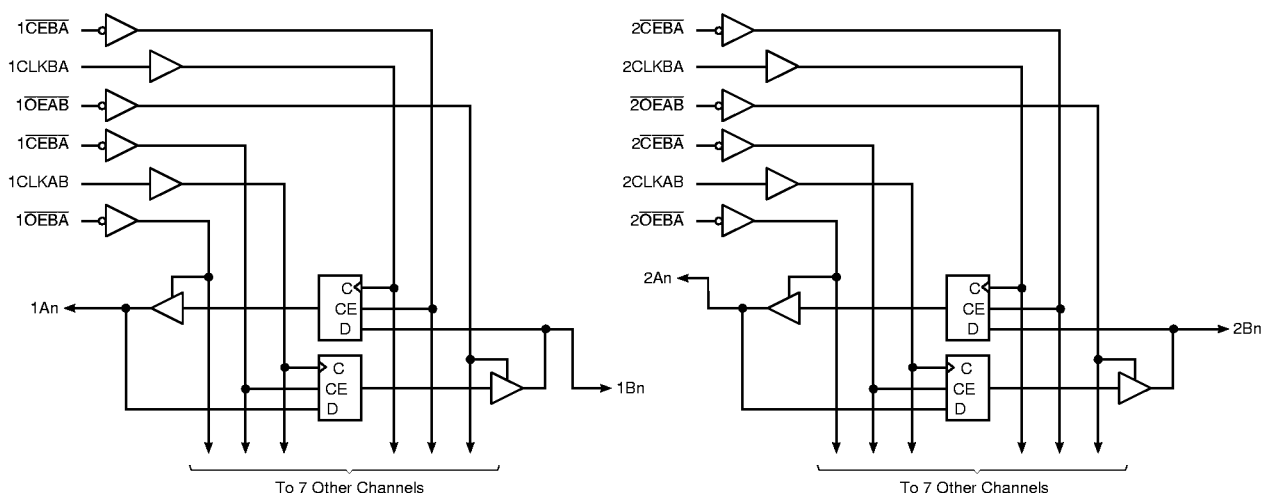# High-Speed CMOS 3.3V 16-Bit Bus Register Transceiver with Bus Hold

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Industry standard pinout
- Bus Hold feature holds last active state during 3-state operation
- 10μA I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V – 3.6V V_{CC} supply operation
- ±24mA balanced output drive
- Meets or exceeds JEDEC Standard 36 specifications
- t_{PD} = 6.3ns
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Operating temperature range:
    –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
    Human body model > 2000V
    Machine model > 200V
- Packages available:
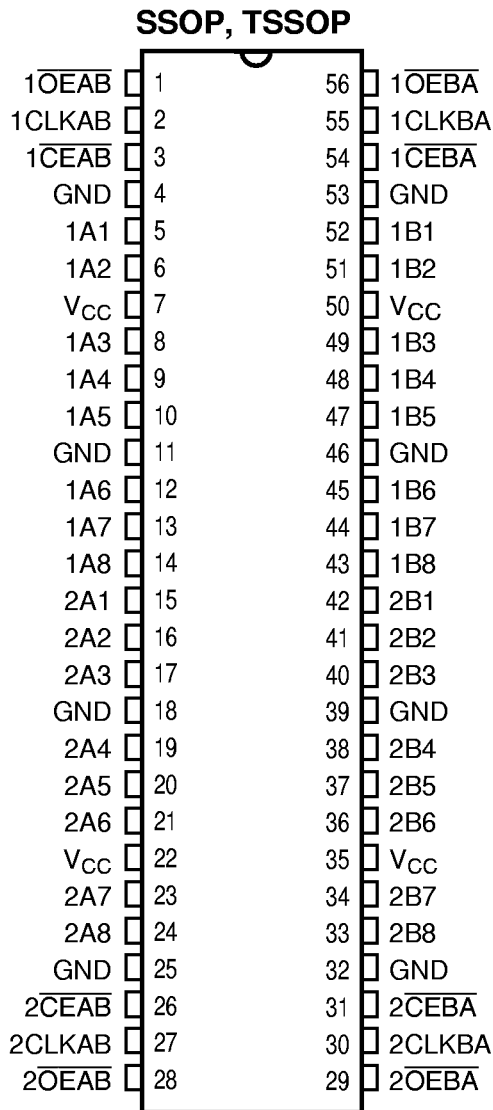   56-pin TSSOP
    56-pin SSOP

DESCRIPTION

The LCX16H952 is a 16-bit bus register transceiver with three-state outputs that is ideal for driving address and data buses. Two independent 8-bit registered transceivers are used to permit independent control of data flow in either direction. The QS74LCX16H952 provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V systems. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

Figure 2. Pin Configuration
(All Pins Top View)

SSOP, TSSOP

1$\overline{\text{OEAB}}$	1	56	1$\overline{\text{OEBA}}$
1CLKAB	2	55	1CLKBA
1$\overline{\text{CEAB}}$	3	54	1$\overline{\text{CEBA}}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V$_{CC}$	7	50	V$_{CC}$
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V$_{CC}$	22	35	V$_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2$\overline{\text{CEAB}}$	26	31	2$\overline{\text{CEBA}}$
2CLKAB	27	30	2CLKBA
2$\overline{\text{OEAB}}$	28	29	2$\overline{\text{OEBA}}$

Table 1. Pin Description

Name	Description
x$\overline{\text{OEAB}}$	A to B Output Enable Inputs (Active LOW)
x$\overline{\text{OEBA}}$	B to A Output Enable Inputs (Active LOW)
x$\overline{\text{CEAB}}$	A to B Enable Inputs (Active LOW)
x$\overline{\text{CEBA}}$	B to A Enable Inputs (Active LOW)
xCLKAB	A to B Clock Inputs
xCLKBA	B to A Clock Inputs
xAx	A to B Data Inputs or B to A 3-State Outputs (Bus Hold Inputs)
xBx	B to A Data Inputs or A to B 3-State Outputs (Bus Hold Inputs)

Table 2. Function Table[1,2]

Inputs				Outputs
x$\overline{\text{CEAB}}$	xCLKAB	x$\overline{\text{OEAB}}$	xAx	xBx
H	X	L	X	B[3]
X	L	L	X	B[3]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

Notes:
1. ↑ = LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown: B-to-A flow control is the same, except using x$\overline{\text{CEBA}}$, xCLKBA, and x$\overline{\text{OEBA}}$.
3. Level of B before the indicated steady-state input conditions were established.

Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C$_{IN}$	Input Capacitance	7.0	pF	V$_{IN}$ = 0V, V$_{OUT}$ = 0V, f = 1MHz
C$_{I/O}$	I/O Capacitance	8.0	pF	V$_{IN}$ = 0V, V$_{OUT}$ = 0V, f = 1MHz
C$_{PD}$	Power Dissipation Capacitance	25	pF	V$_{CC}$ = 3.3V, V$_{IN}$ = 0 or V$_{CC}$, f = 10MHz

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground .... −0.5V to 7.0V
DC Output Voltage V_{OUT}
     Outputs HIGH-Z .... −0.5V to 7.0V
     Outputs Active .... −0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} .... −0.5V to 7.0V
DC Input Diode Current with V_{IN} < 0 .... −50mA
DC Output Diode Current
     V_O < 0 .... −50mA
     V_O > V_{CC} 50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) .... ±50mA
DC Supply Current per Supply Pin .... ±100mA
DC Ground Current per Ground Pin .... ±100mA
T_{STG} Storage Temperature .... −65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, Operating		2.0	3.6	V
	Supply Voltage, Data Retention		1.5	3.6	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage in Active State		0	V_{CC}	V
	Output Voltage in "OFF" State		0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0 − 3.6V	—	±24	mA
		V_{CC} = 2.7V	—	±12	
Δt/Δv	Input Transition Slew Rate		—	10	ns/V
T_A	Operating Free Air Temperature		−40	85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, $T_A = -40°C$ to $85°C$.

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs		—	—	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7V, I_{OH} = -100\mu A$		$V_{CC} - 0.2$	—	—	V
		$V_{CC} = 2.7V, I_{OH} = -12mA$		2.2	—	—	
		$V_{CC} = 3.0V, I_{OH} = -18mA$		2.4	—	—	
		$V_{CC} = 3.0V, I_{OH} = -24mA$		2.2	—	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7V, I_{OL} = 100\mu A$		—	—	0.2	V
		$V_{CC} = 2.7V, I_{OL} = 12mA$		—	—	0.4	
		$V_{CC} = 3.0V, I_{OL} = 16mA$		—	—	0.4	
		$V_{CC} = 3.0V, I_{OL} = 24mA$		—	—	0.5	
ΔV_T	Input Hysteresis[3]	$V_{TLH} - V_{THL}$ for All Inputs		—	150	—	mV
I_I	Input Leakage Current	$V_{CC} = 3.6V, V_I = 0V, V_I = 5.5V$		—	—	±1.0	μA
| I_{BH} |	Input Current Inputs High or Low Bus Hold Inputs[3,4]	$V_{CC} = 3.6V, V_{IN} = 0V$ or $V_{IN} = V_{CC}$		—	—	50	μA
		$V_{CC} = 3.6V, 0.8V < V_{IN} < 2.0V$		—	—	500[5]	μA
I_{BHH}	Bus Hold Sustaining Current	$V_{CC} = 3.0V$	$V_{IN} = 2.0V$	−75	—	—	μA
I_{BHL}	Bus Hold Inputs		$V_{IN} = 0.8V$	75	—	—	μA
I_{OZ}	High-Z I/O Leakage[3]	$V_O = 0V, V_O = 5.5V,$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6V$		—	—	±1.0	μA
I_{OFF}	Power Off Leakage	$V_{CC} = 0V, V_I$ or $V_O = 5.5V$		—	—	10	μA
I_{OS}	Short Circuit Current[3,6]	$V_{CC} = 3.6V, V_{OUT} = GND$		−60	—	−200	mA
V_{IK}	Input Clamp Voltage	$V_{CC} = 2.7V, I_{IN} = -18$ mA		—	−0.7	−1.2	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$ and $T_A = 25°C$.
3. These parameters are guaranteed by characterization, but not production tested.
4. Pins with Bus Hold are identified in the Pin Description.
5. An external driver must provide at least | I_{BH} | during transition to guarantee that the Bus Hold input will change state.
6. Not more than one output should be tested at one time. Duration of test should not exceed one second.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[1]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, Freq = 0, V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.6V, V_{IN} = V_{CC} −0.6V	Control Inputs	2.0	30	µA
			Bus Hold Inputs	—	500	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycling x$\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	65	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycle f = 5MHz, f_{CP} = 10MHz (xCLKAB) x$\overline{OEAB}$ = x$\overline{CEAB}$ = GND x$\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} −0.6V V_{IN} = GND	0.5[5]	1.0[5]	mA
		V_{CC} = 3.6V, Outputs Open Sixteen Bits Toggling @ 50% Duty Cycling f = 2.5MHz, f_{CP} = 10MHz (xCLKAB) x$\overline{OEAB}$ = x$\overline{CEAB}$ = GND x$\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} −0.6V V_{IN} = GND	2.7[5]	8.0[5]	mA

Notes:
1. For conditions shown as Min. or Max. use the appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, 25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in total power supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = V_{CC} −0.6V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f = Average Switching Frequency per Output.
   N_O = Number of Outputs Switching.

Table 8. Dynamic Switching Characteristics[1]

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Note: 1. Characterized but not production tested.

Table 9. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = −40°C to 85°C.
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	V_{CC} = 3.3 ±0.3V		V_{CC} = 2.7V[2]		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay xCLKAB, xCLKBA to xAx, xBx	2.0	6.3	2.0	7.3	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx	1.5	7.0	1.5	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx	1.5	6.5	1.5	7.5	ns
t_{SU}	Setup Time HIGH or LOW xAx, xBx to xCKLAB, xCKLBA	2.5	—	2.5	—	ns
t_{H}	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA	1.5	—	1.5	—	ns
t_{SU}	Setup Time HIGH or LOW x$\overline{CEBA}$, x$\overline{CEAB}$ to xCLKAB, xCLKBA	3.0	—	3.0	—	ns
t_{H}	Setup Time HIGH or LOW x$\overline{CEBA}$, x$\overline{CEAB}$ to xCLKAB, xCLKBA	2.0	—	2.0	—	ns
t_{W}	Pulse Width LOW xCLKAB to xCLKBA[2]	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[3]	—	0.5	—	—	ns

Notes:
1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction.
   This parameter is guaranteed by characterization but not production tested.
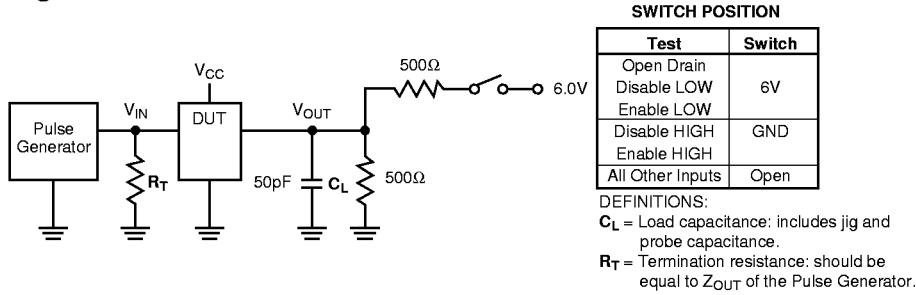
TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit

Pulse Generator — V_{IN} — R_T — DUT — V_{CC} — V_{OUT} — 50pF C_L — 500Ω — 500Ω — 6.0V

SWITCH POSITION

Test	Switch
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

Data Input — t_{REM} — t_H — 3V, 1.5V, 0V

Timing Input — 3V, 1.5V, 0V

Asychronous Control Preset, Clear, Etc. — t_{REM} — 3V, 1.5V, 0V

Sychronous Control Preset, Clear, Clock Enable, Etc. — t_{SU} — t_H — 3V, 1.5V, 0V

Figure 6. Pulse Width

Low-High-Low Pulse — t_W — 1.5V

High-Low-High Pulse — 1.5V
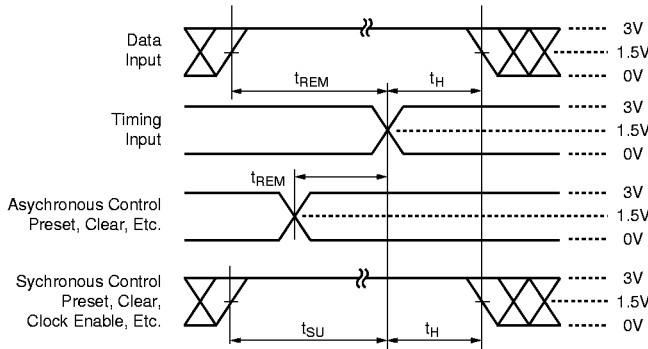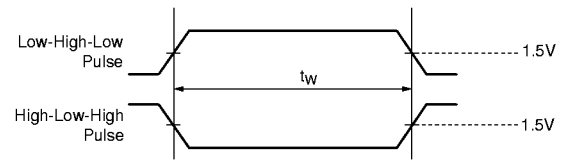
Figure 5. Enable and Disable Timing

Control Input — 3V, 1.5V, 0V

t_{PZL}

Output Normally Low — 3.0V — Switch Closed — 1.5V — 3.0V — 0.3V V_{OL}

t_{PZL} — Switch Open — 1.5V — 0.3V V_{OH}

Output Normally High — 0V — V_{OH} — 0V

Figure 7. Propagation Delay

Same Phase Input Transition — t_{PLH} — t_{PHL} — 3V, 1.5V, 0V

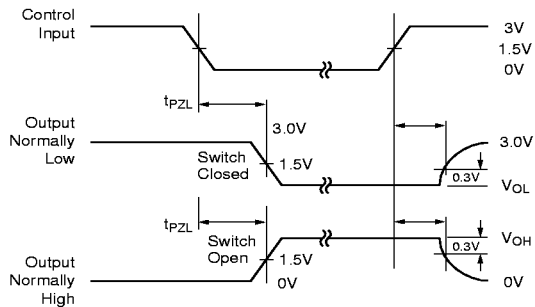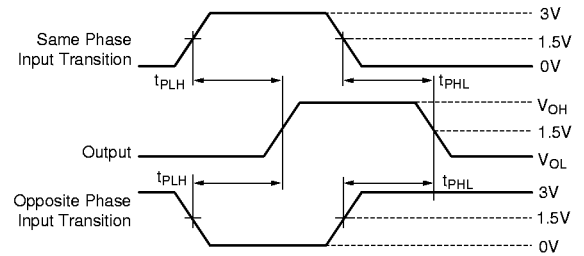Output — t_{PLH} — t_{PHL} — V_{OH}, 1.5V, V_{OL}

Opposite Phase Input Transition — 3V, 1.5V, 0V

Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_F, t_R ≤ 2.5ns.

ORDERING INFORMATION

QS74LCX　　XX　　XX　　XXX　　X　　XX

- Package Type
- Speed Grade
- Device Type
- Feature Selection
- Number of Bit
- −40°C to 85°C

Device Type:
952

Speed Grades:
Blank – Standard

Package Type:
PV – SSOP, 300 mil

PA – TSSOP, 240 mil

Feature Selection:
H – Bus Hold

Number of Bit:
16 – 16-Bit

300-MIL SSOP - Package Code PV
**Shrink Small Outline Package**
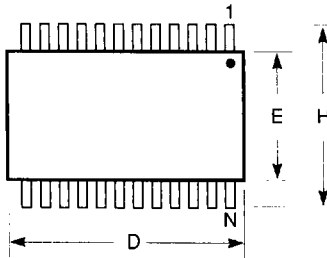**Plastic Small Outline Gull-Wing**
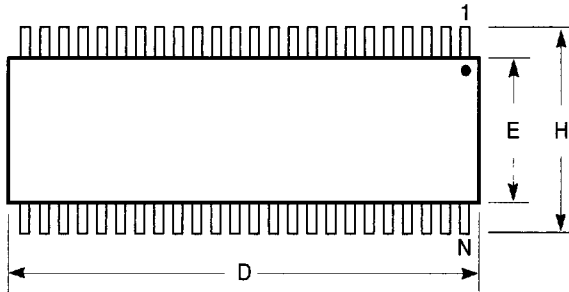
Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.
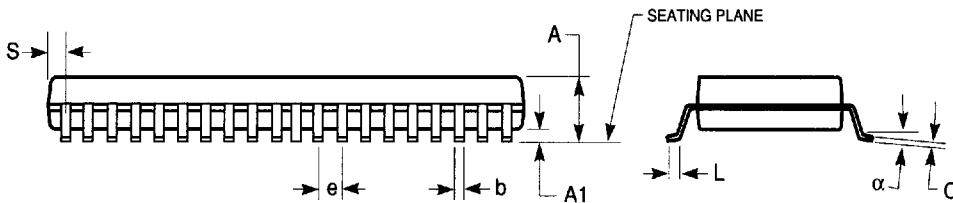
JEDEC#	MO-118AA			MO-118AB		
DWG#	PSS-48B			PSS-56B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.095	0.102	0.110	0.095	0.102	0.110
A1	0.008	0.012	0.016	0.008	0.012	0.016
b	0.008	0.010	0.0135	0.008	0.010	0.0135
C	0.005	0.008	0.010	0.005	0.008	0.010
D	0.620	0.625	0.630	0.720	0.725	0.730
E	0.291	0.295	0.299	0.291	0.295	0.299
e	0.025 BSC			0.025 BSC		
H	0.395	0.410	0.420	0.395	0.410	0.420
L	0.020	0.030	0.040	0.020	0.030	0.040
N	48			56		
α	0°	5°	8°	0°	5°	8°
S	0.022	0.025	0.028	0.022	0.025	0.028

170-MIL TSSOP - Package Code PA
Thin Shrink Small Outline Package
Plastic Small Outline Gull-Wing
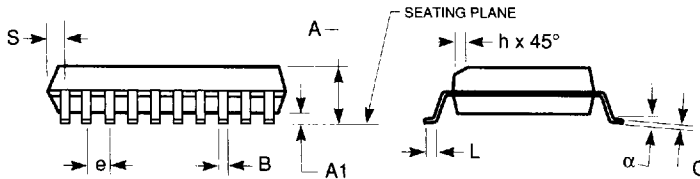
Notes:
1. Refer to applicable symbol list.
2. N is the number of lead positions.
3. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
4. Lead coplanarity is 0.004in. maximum.

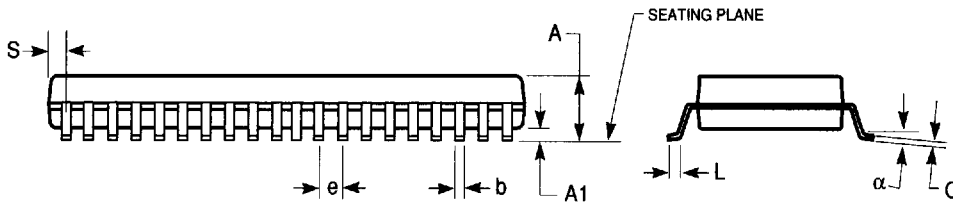| JEDEC#	MO-153AD			MO-153AD		
DWG#	PSS-24C			PSS-24C		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.045	0.046	0.047	1.14	1.17	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
b	0.007	0.010	0.012	0.19	0.25	0.30
C	0.004	0.005	0.006	0.09	0.13	0.16
D	0.303	0.307	0.311	7.7	7.8	7.9
E	0.169	0.173	0.177	4.3	4.4	4.5
e	0.025 BSC			0.65 BSC		
H	0.238	0.252	0.269	6.1	6.4	6.7
L	0.020	0.024	0.030	0.50	0.60	0.75
N	24			24		
α	0°	5°	8°	0°	5°	8°
S	0.007	0.008	0.009	0.18	0.2	0.22

IN INCHES   IN MILLIMETERS

Q QUALITY
SEMICONDUCTOR, INC.

240-MIL TSSOP - Package Code PA
Thin Shrink Small Outline Package
Plastic Small Outline Gull-Wing
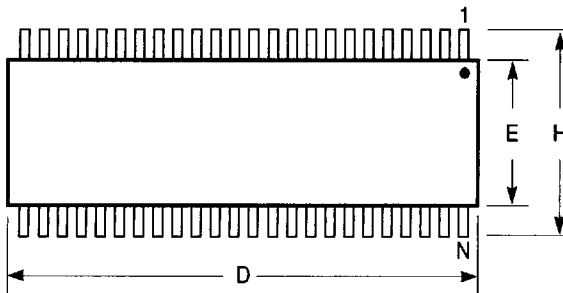
Notes:
1. Refer to applicable symbol list.
2. N is the number of lead positions.
3. Dimensions D, E, and S are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
4. Lead coplanarity is 0.004in. maximum.

JEDEC#	MO-153ED			MO-153EE			MO-153ED			MO-153EE		
DWG#	PSS-48C			PSS-56C			PSS-48C			PSS-56C		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.039	0.043	0.047	0.039	0.043	0.047	1.00	1.10	1.20	1.00	1.10	1.20
A1	0.002	0.004	0.006	0.002	0.004	0.006	0.05	0.10	0.15	0.05	0.10	0.15
b	0.006	0.008	0.011	0.006	0.008	0.011	0.17	0.20	0.27	0.17	0.20	0.27
C	0.004	0.006	0.008	0.004	0.006	0.008	0.09	0.15	0.20	0.09	0.15	0.20
D	0.488	0.492	0.496	0.547	0.551	0.555	12.40	12.50	12.60	13.90	14.00	14.10
E	0.236	0.240	0.244	0.236	0.240	0.244	6.00	6.10	6.20	6.00	6.10	6.20
e	0.0197 BSC			0.0197 BSC			0.50 BSC			0.50 BSC		
H	0.315	0.319	0.323	0.315	0.319	0.323	8.00	8.10	8.20	8.00	8.10	8.20
L	0.018	0.024	0.030	0.018	0.024	0.030	0.45	0.60	0.75	0.45	0.60	0.75
N	48			56			48			56		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.015	0.020	0.025	0.006	0.010	0.014	0.38	0.50	0.65	0.15	0.25	0.35

DIMENSIONS IN INCHES   DIMENSIONS IN MILLIMETERS

■ 7466803 0003757 T87 ■