- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.25 V (Min) at 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise . . . 16 nV/√Hz Typ at f = 1 kHz**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLV2442A)
- **Low Input Bias Current . . . 1 pA Typ**
- **600-Ω Output Drive**
- **High-Gain Bandwidth . . . 1.8 MHz Typ**
- **Low Supply Current . . . 750 μA Per Channel Typ**
- **Macromodel Included**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV2442 and TLV2442A are dual low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range of these devices has been extended over typical standard CMOS amplifiers, making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. Both devices offer comparable ac performance while having lower noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLV2442 has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecommunications applications.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

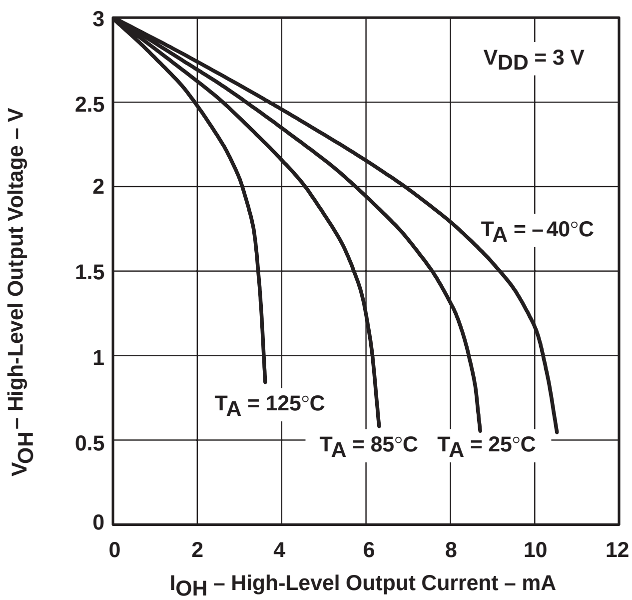


Figure 1

The other members in the TLV2442 family are the low-power, TLV2432, and micro-power, TLV2422, versions.

The TLV2442, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV2442A is available with a maximum input offset voltage of 950 μV.

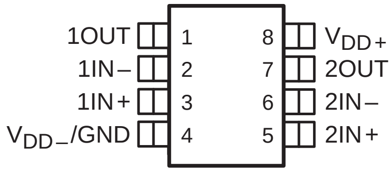
If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

AVAILABLE OPTIONS

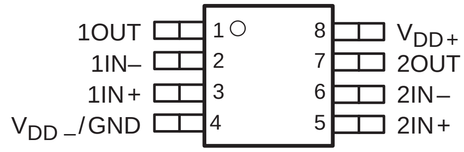
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	2.5 mV	TLV2442CD	—	—	TLV2442CPWLE	—
–40°C to 85°C	950 µV 2.5 mV	TLV2442AID TLV2442ID	— —	— —	TLV2442AIPWLE —	— —
–40°C to 125°C	950 µV 2.5 mV	TLV2442AQD TLV2442QD	— —	— —	— —	— —
–55°C to 125°C	950 µV 2.5 mV	— —	TLV2442AMFK TLV2442MFK	TLV2442AMJG TLV2442MJG	— —	TLV2442AMU TLV2442MU

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2442CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

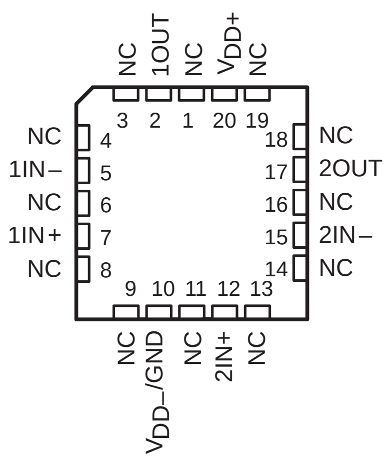
D OR JG PACKAGE (TOP VIEW)



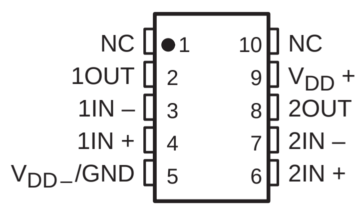
PW PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)

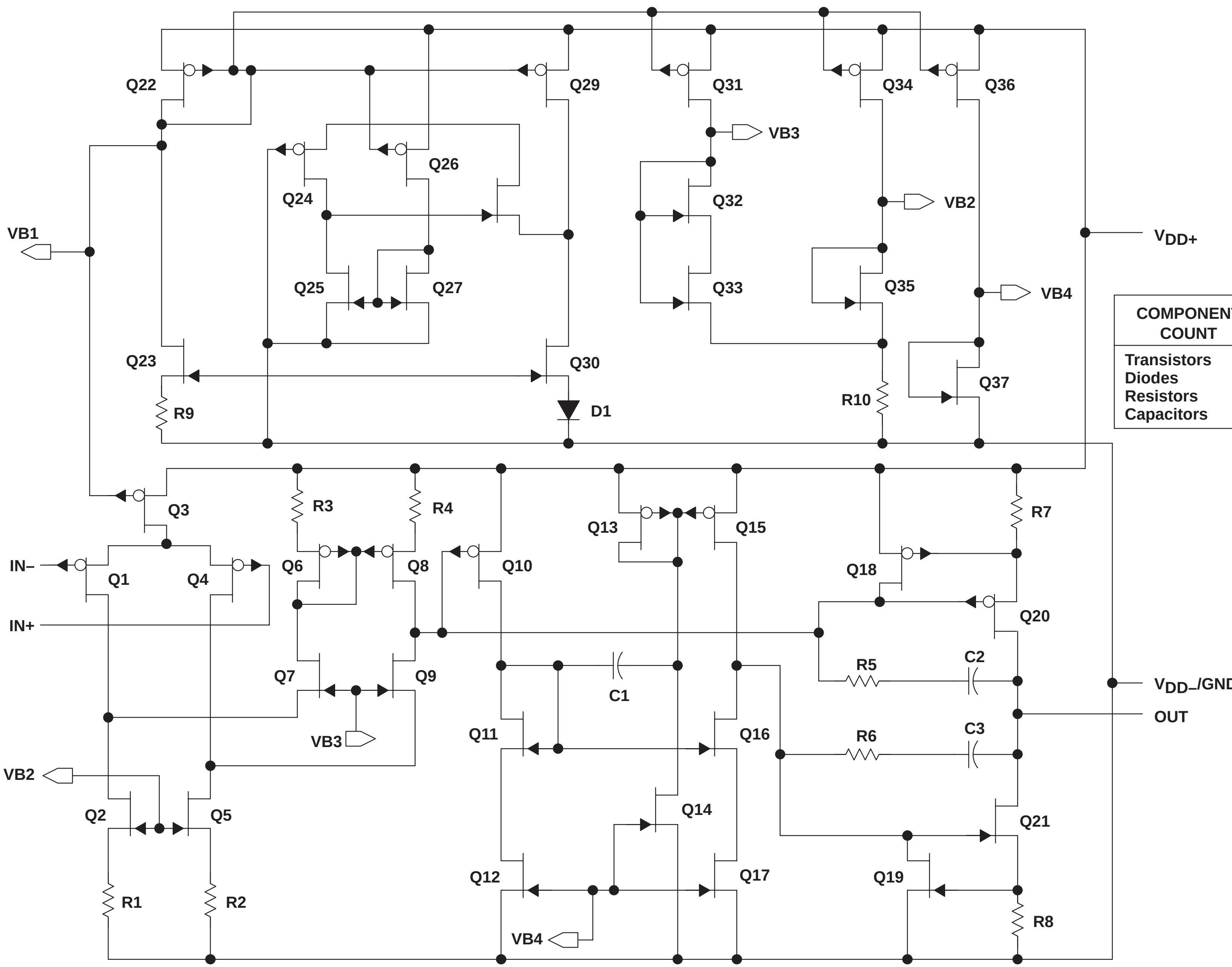


U PACKAGE (TOP VIEW)



NC – No internal connection

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1) . . . . . –0.3 V to V_{DD}
Input current, I_I (any input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Q suffix . . . . . –40°C to 125°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	V_{DD+} – 1.0	V_{DD-}	V_{DD+} – 1.0	V_{DD-}	V_{DD+} – 1.3	V_{DD-}	V_{DD+} – 1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} – 1.0	V_{DD-}	V_{DD+} – 1.0	V_{DD-} + 2	V_{DD+} – 1.3	V_{DD-} + 2	V_{DD+} – 1.3	V
Operating free-air temperature, T_A	0	70	–40	85	–40	125	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C MIN	TLV2442C TYP	TLV2442C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		300	2000	μV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV,	R_S = 50 Ω	25°C	0 to 2.25	–0.25 to 2.5		V
				Full range	0 to 2			
V_{OH}	High-level output voltage	I_O = –100 μA		25°C		2.98		V
		I_O = –3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_O = 100 μA	25°C		0.02		V
		V_{IC} = 0,	I_O = 3 mA	25°C		0.63		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω	25°C	0.7	1		V/mV
				Full range	0.4			
			R_L = 1 MΩ	25°C		750		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	65	75		dB
				Full range	55			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		1.5	2.2	mA
				Full range			2.2	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2442I MIN	TLV2442I TYP	TLV2442I MAX	TLV2442AI MIN	TLV2442AI TYP	TLV2442AI MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2000		300	950	μV
			Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert$ ≤ 5 mV, R_S = 50 Ω	25°C	0 to 2.25	–0.25 to 2.5		0 to 2.25	–0.25 to 2.5		V
			Full range	0 to 2			0 to 2			
V_{OH}	High-level output voltage	I_O = –100 μA	25°C		2.98			2.98		V
		I_O = –3 mA	25°C		2.5			2.5		
			Full range	2.25			2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0, I_O = 100 μA	25°C		0.02			0.02		V
		V_{IC} = 0, I_O = 3 mA	25°C		0.63			0.63		
			Full range			1			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V, R_L = 600 Ω	25°C	0.7	1		0.7	1		V/mV
			Full range	0.4			0.4			
		V_O = 1 V to 2 V, R_L = 1 MΩ	25°C		750			750		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, V_O = 1.5 V, R_S = 50 Ω	25°C	65	75		65	75		dB
			Full range	55			55			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = $V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		1.45	2.2		1.45	2.2	mA
			Full range			2.2			2.2	

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C, TLV2442I TLV2442AI MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 600 Ω, C_L = 100 pF		25°C	0.65	1.3		V/µs
				Full range	0.65			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		170		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.6		µV
		f = 0.1 Hz to 10 Hz		25°C		5.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.08%		
			A_V = 10			0.3%		
			A_V = 100			2%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω, A_V = 1, C_L = 100 pF		25°C		0.9		MHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%	25°C		1.5		µs
			To 0.01%			3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		65°		
	Gain margin			25°C		9		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is –40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2442Q, TLV2442M			TLV2442AQ, TLV2442AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C		300	2000		300	950	µV
			Full range			2500			1600	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			260			260	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV, R_S = 50 Ω	25°C to –55°C	0 to 2.25	–0.25 to 2.5		0 to 2.25	–0.25 to 2.5		V
			125°C	0.2 to 2			0.2 to 2			
V_{OH}	High-level output voltage	I_O = –100 µA	25°C		2.98			2.98		V
		I_O = –3 mA	25°C		2.5			2.5		
			Full range	2.25			2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0, I_O = 100 µA	25°C		0.02			0.02		V
		V_{IC} = 0, I_O = 3 mA	25°C		0.63			0.63		
			Full range			1			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V, R_L = 600 Ω‡	25°C	0.7	1		0.7	1		V/mV
			Full range	0.4			0.4			
		V_{IC} = 1.5 V, V_O = 1 V to 2 V, R_L = 1 MΩ‡	25°C		750			750		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} MIN, V_O = 1.5 V, R_S = 50 Ω	25°C	65	75		65	75		dB
			Full range	50			50			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = $V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		1.45	2.2		1.45	2.2	mA
			Full range			2.2			2.2	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 1.5 V.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442Q, TLV2442M, TLV2442AQ, TLV2442AM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 600 Ω, C_L = 100 pF		25°C	0.65	1.3		V/µs
				Full range	0.4			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		170		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.6		µV
		f = 0.1 Hz to 10 Hz		25°C		5.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.08%		
			A_V = 10			0.3%		
			A_V = 100			2%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω, A_V = 1, C_L = 100 pF		25°C		0.9		MHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%	25°C		1.5		µs
			To 0.01%			3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		65°		
	Gain margin			25°C		9		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C MIN	TLV2442C TYP	TLV2442C MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2000	µV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	25°C	0 to 4.25	–0.25 to 4.5		V
				Full range	0 to 4			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 µA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 600 Ω‡	25°C	0.9	1.3		V/mV
				Full range	0.5			
			R_L = 1 MΩ‡	25°C		950		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.25 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	75		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		1.5	2.2	mA
				Full range			2.2	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2442I MIN	TLV2442I TYP	TLV2442I MAX	TLV2442AI MIN	TLV2442AI TYP	TLV2442AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2000		300	950	µV
			Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV, R_S = 50 Ω	25°C	0 to 4.25	–0.25 to 4.5		0 to 4.25	–0.25 to 4.5		V
			Full range	0 to 4			0 to 4			
V_{OH}	High-level output voltage	I_{OH} = –100 µA	25°C		4.97			4.97		V
		I_{OH} = –5 mA	25°C	4	4.35		4	4.35		
			Full range	4			4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.8			0.8		
			Full range			1.25			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 600 Ω‡	25°C	0.9	1.3		0.9	1.3		V/mV
			Full range	0.5			0.5			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		950			950		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.25 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.5	2.2		1.5	2.2	mA
			Full range			2.2			2.2	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C, TLV2442I TLV2442AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.4		V/µs
				Full range	0.75			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		130		nV/√Hz
		f = 1 kHz		25°C		16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.8		µV
		f = 0.1 Hz to 10 Hz		25°C		3.6		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.17%		
			A_V = 100			1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		0.5		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		µs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡, C_L = 100 pF‡		25°C		68°		
	Gain margin			25°C		8		dB

† Full range for the C suffix is 0°C to 70°C. Full range for the I suffix is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2442Q, TLV2442M MIN	TLV2442Q, TLV2442M TYP	TLV2442Q, TLV2442M MAX	TLV2442AQ, TLV2442AM MIN	TLV2442AQ, TLV2442AM TYP	TLV2442AQ, TLV2442AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2000		300	950	µV
			Full range			2500			1600	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			260			260	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV, R_S = 50 Ω	25°C	0 to 4.25	–0.25 to 4.5		0 to 4.25	–0.25 to 4.5		V
			Full range	0 to 4			0 to 4			
V_{OH}	High-level output voltage	I_{OH} = –100 µA	25°C		4.97			4.97		V
		I_{OH} = –5 mA	25°C	4	4.35		4	4.35		
			Full range	4			4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.8			0.8		
			Full range			1.25			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 600 Ω‡	25°C	0.9	1.3		0.9	1.3		V/mV
			Full range	0.5			0.5			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		950			950		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} MIN, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.5	2.2		1.5	2.2	mA
			Full range			2.2			2.2	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442Q, TLV2442M, TLV2442AQ, TLV2442AM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 4 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.4		V/μs
				Full range	0.5			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		130		nV/√Hz
		f = 1 kHz		25°C		16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.8		μV
		f = 0.1 Hz to 10 Hz		25°C		3.6		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.17%		
			A_V = 100			1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		0.5		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		μs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡, C_L = 100 pF‡		25°C		68°		
	Gain margin			25°C		8		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs†

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	2, 3 4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_{OH}	High-level output voltage	vs High-level output current	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	14 15
V_O	Output voltage	vs Differential Input voltage	16, 17
A_{VD}	Differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	18 19, 20 21, 22
z_o	Output impedance	vs Frequency	23, 24
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	25 26
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	27, 28 29
I_{DD}	Supply current	vs Supply voltage	30
SR	Slew rate	vs Load capacitance vs Free-air temperature	31 32
V_O	Inverting large-signal pulse response	vs Time	33, 34
	Voltage-follower large-signal pulse response	vs Time	35, 36
	Inverting small-signal pulse response	vs Time	37, 38
	Voltage-follower small-signal pulse response	vs Time	39, 40
V_n	Equivalent input noise voltage	vs Frequency	41, 42
	Noise voltage	Over a 10-second period	43
THD + N	Total harmonic distortion plus noise	vs Frequency	44, 45
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	46 47
ϕ_m	Phase margin	vs Frequency vs Load capacitance	19, 20 48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

† For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

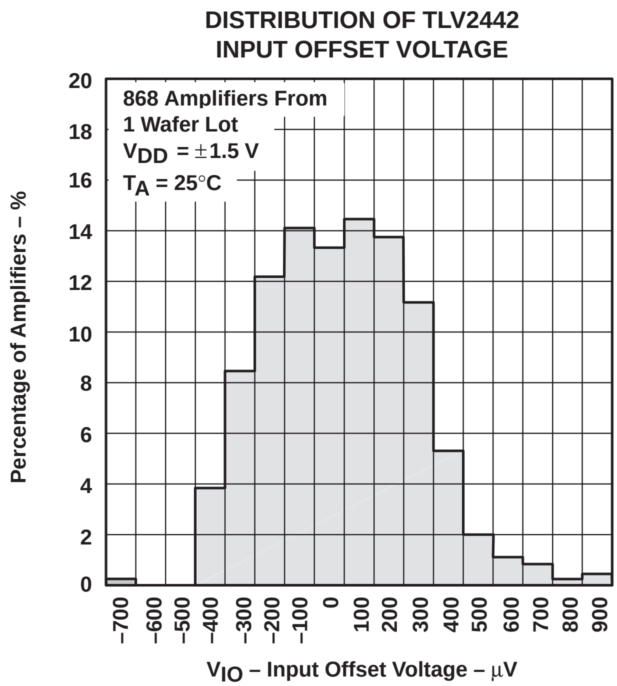


Figure 2

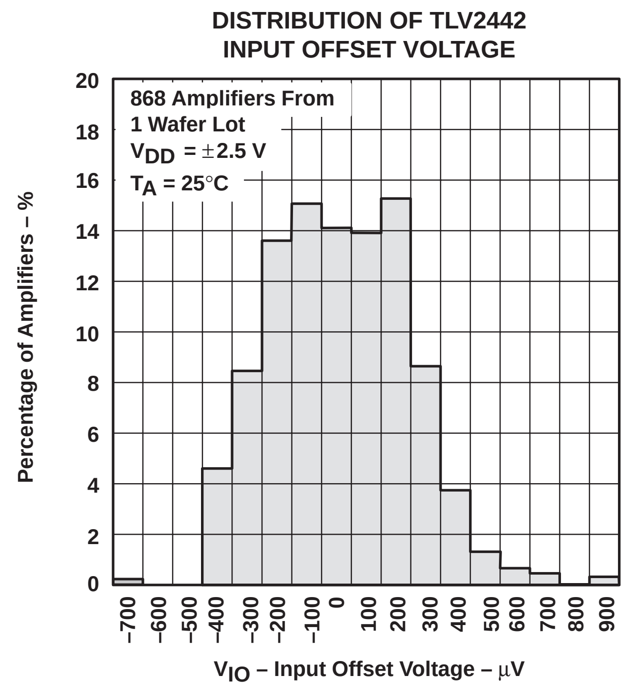


Figure 3

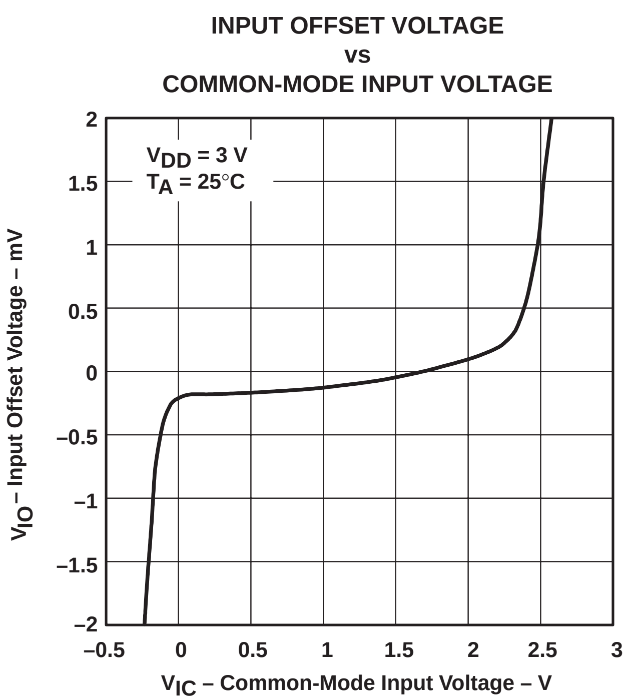


Figure 4

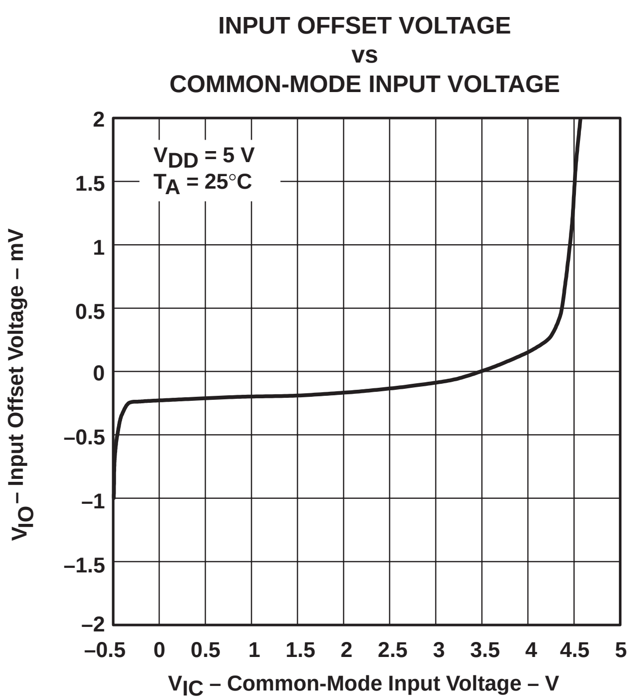


Figure 5

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

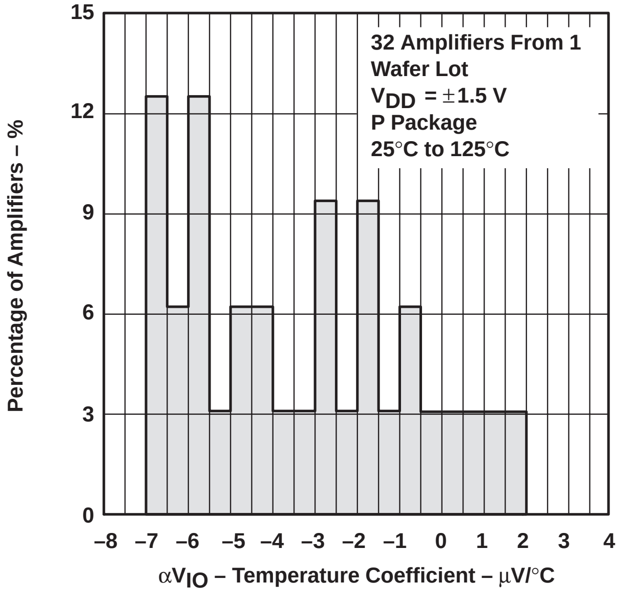


Figure 6

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

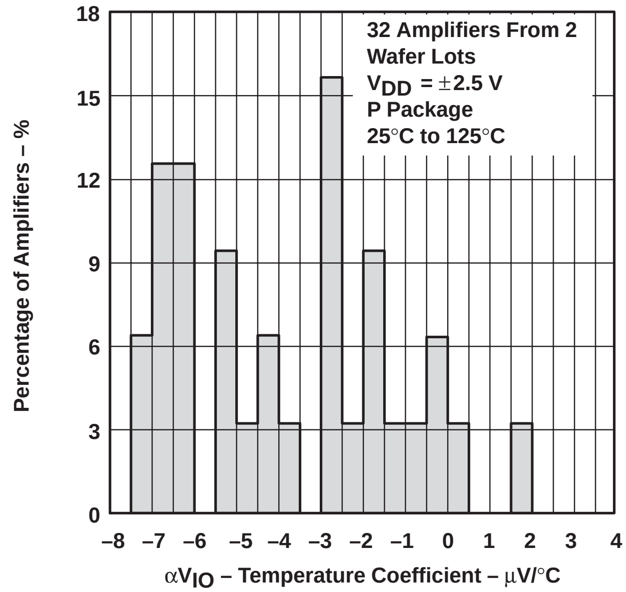


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

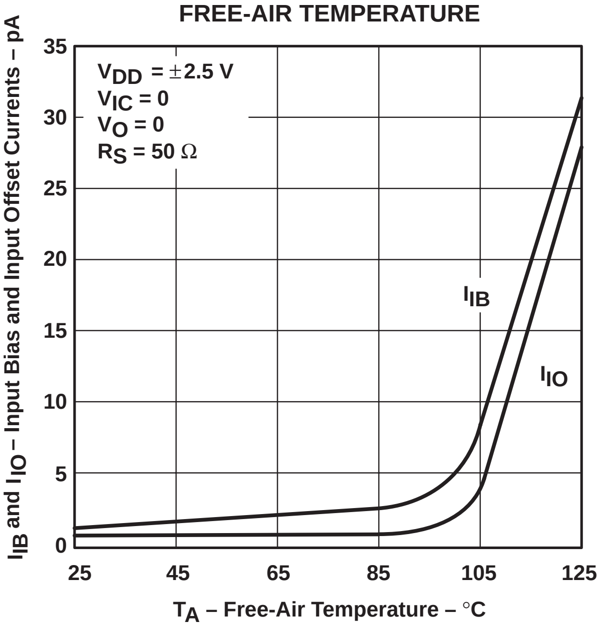


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

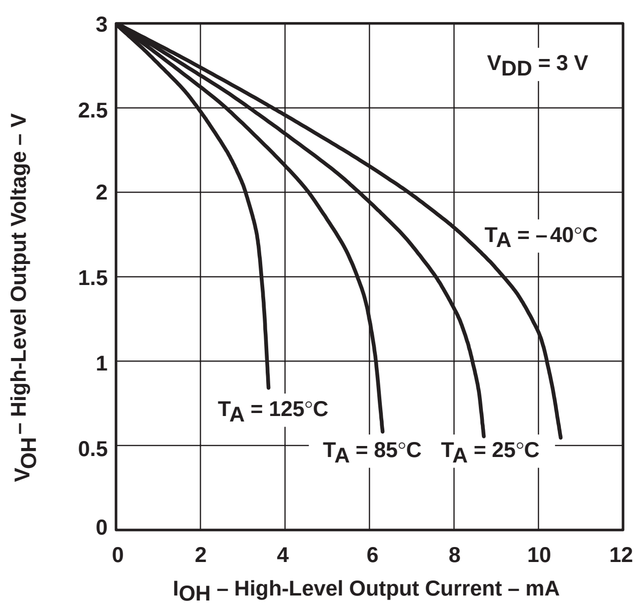


Figure 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

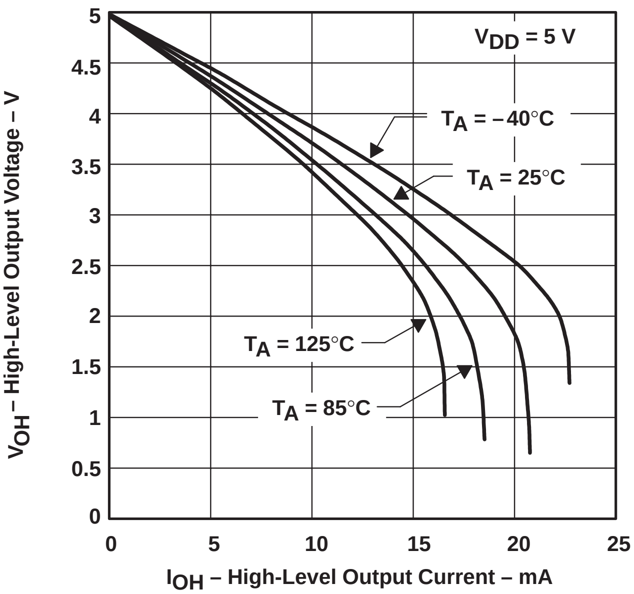


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

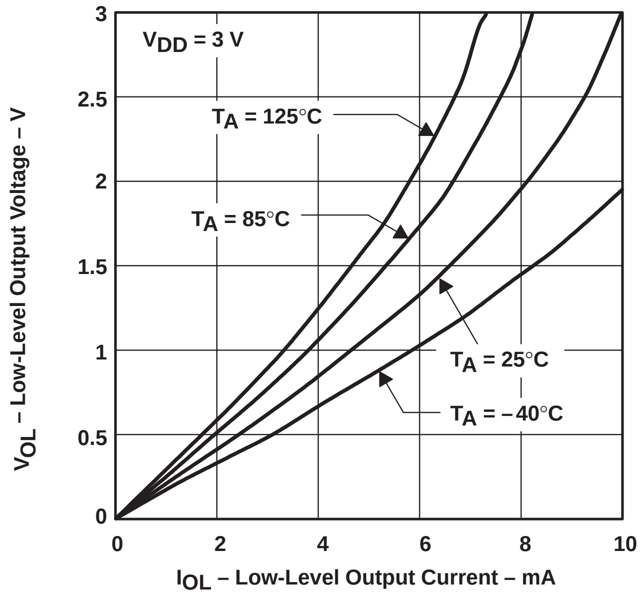


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

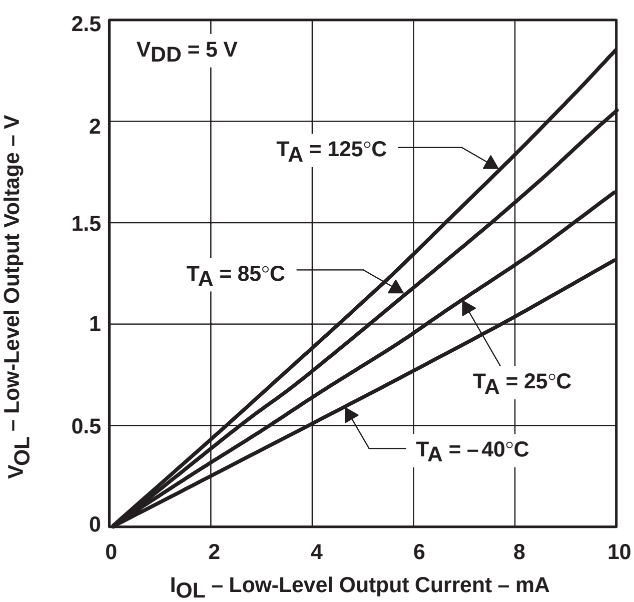


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

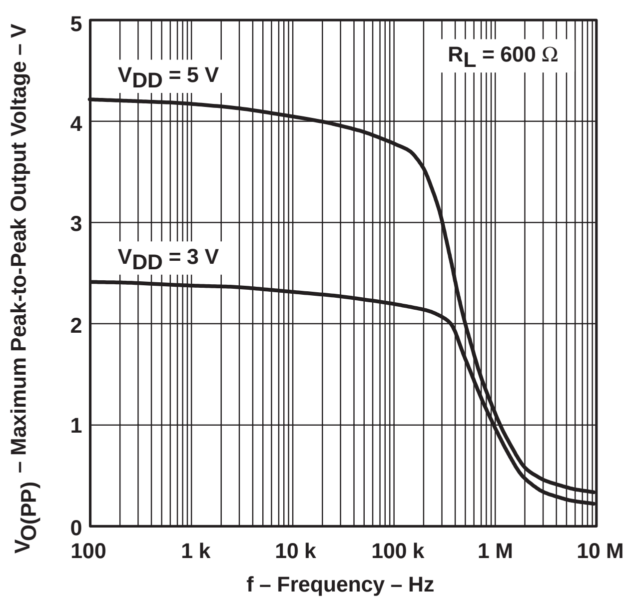


Figure 13

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

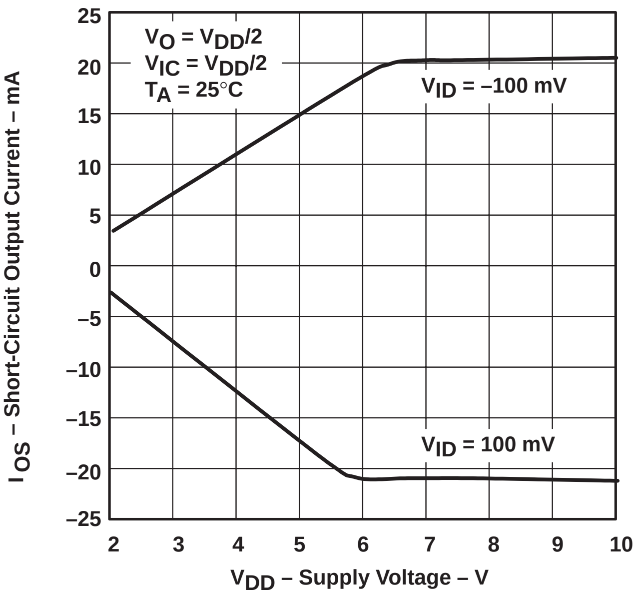


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

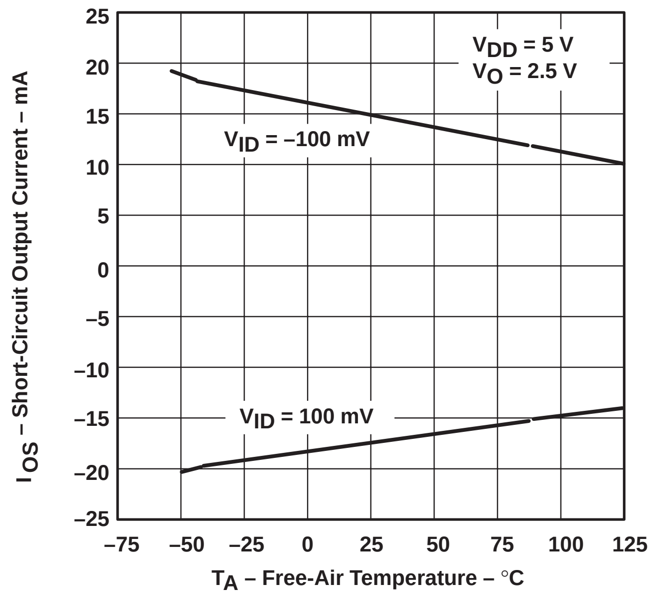


Figure 15

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

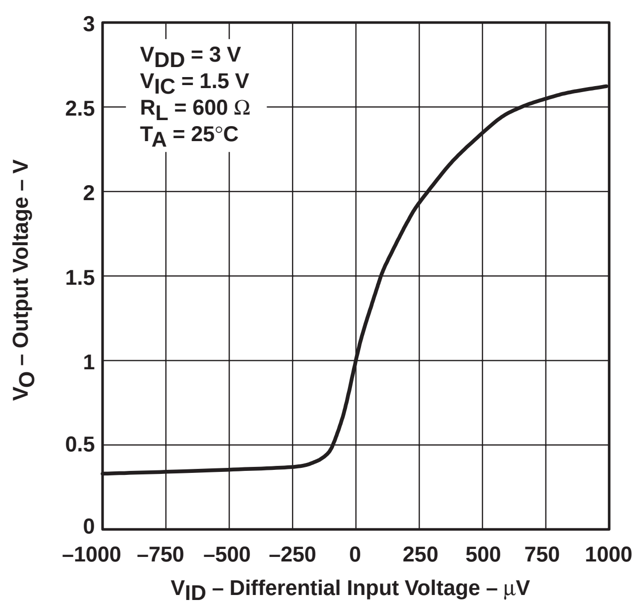


Figure 16

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

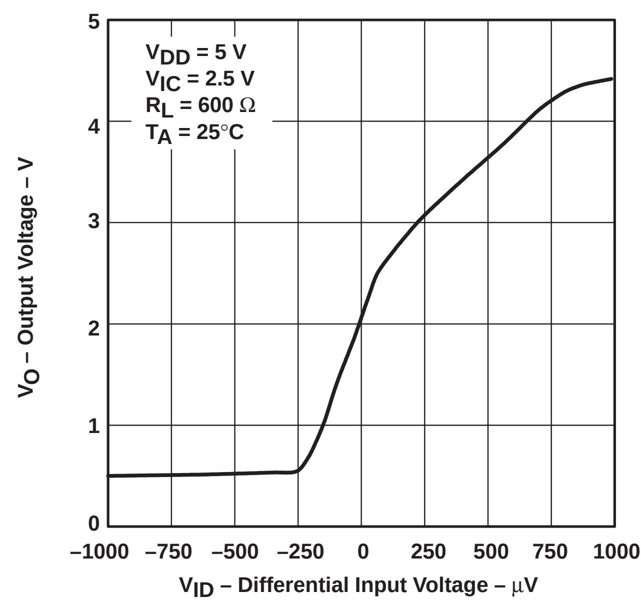


Figure 17

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

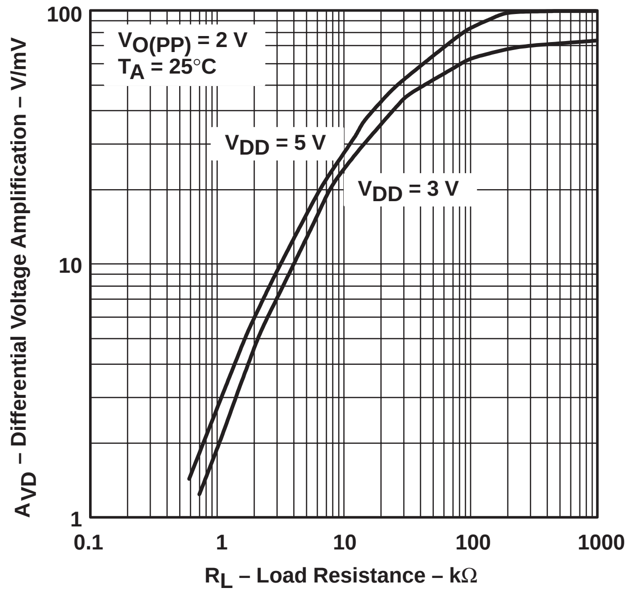


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

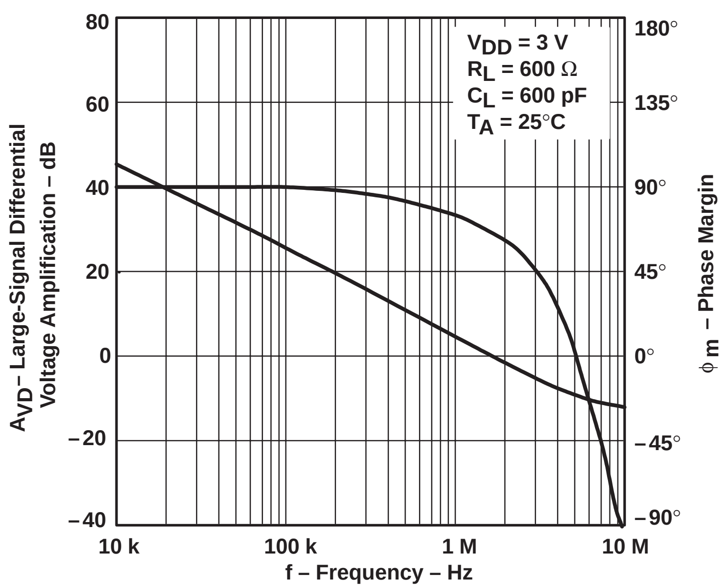


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

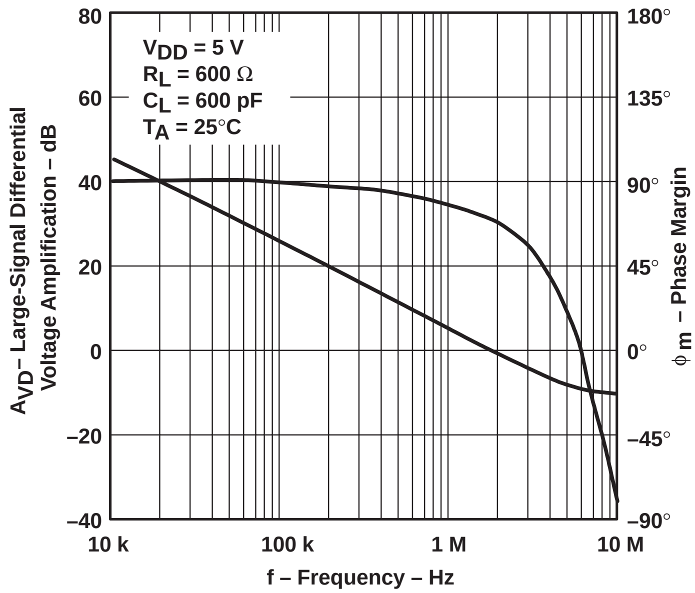


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

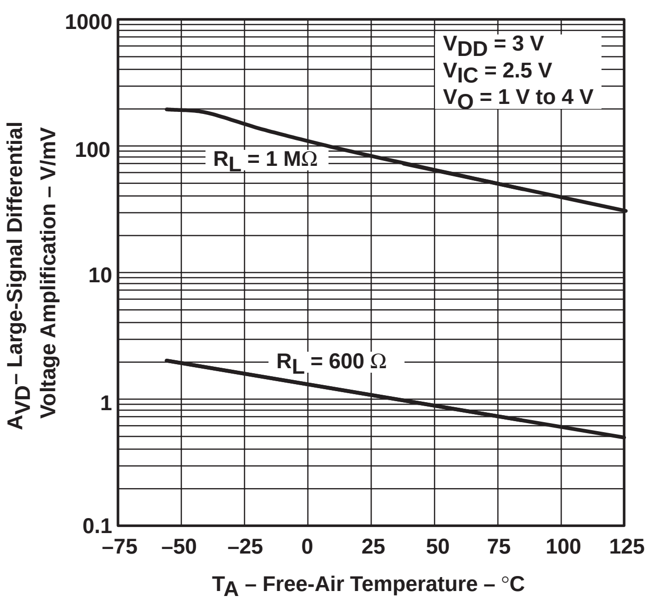


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

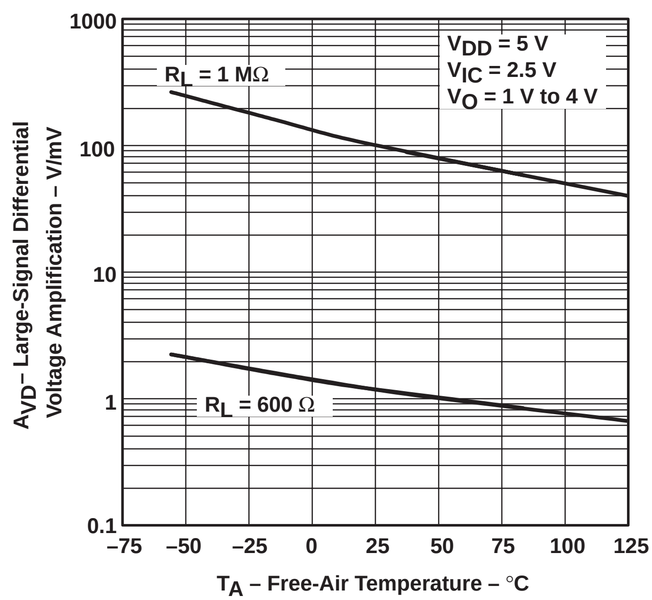


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

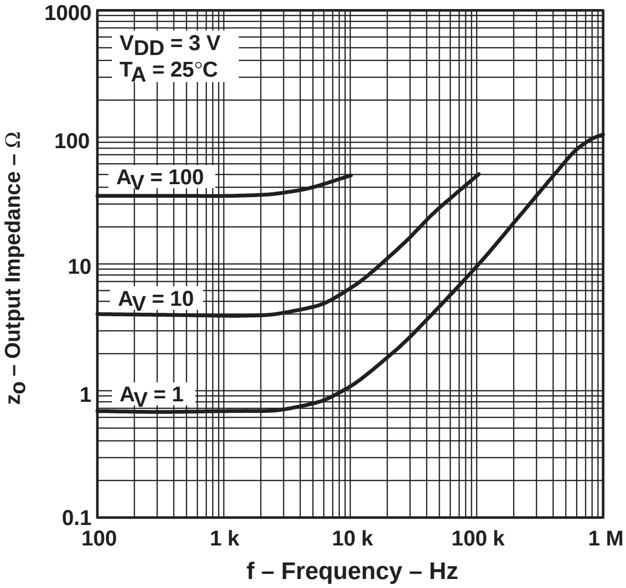


Figure 23

OUTPUT IMPEDANCE
vs
FREQUENCY

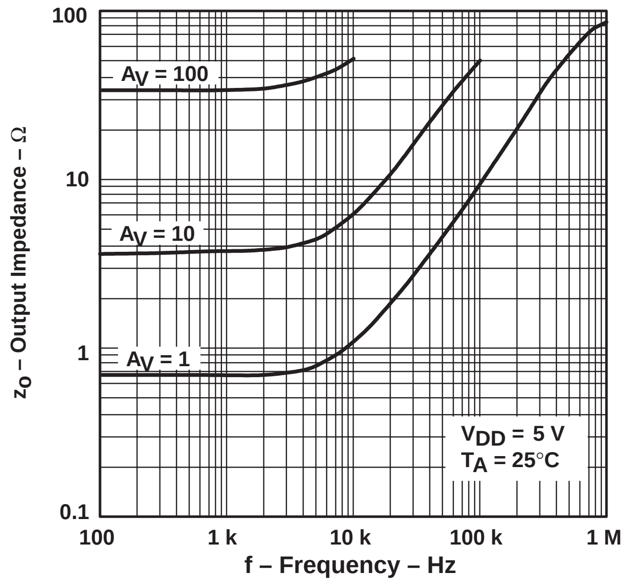


Figure 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

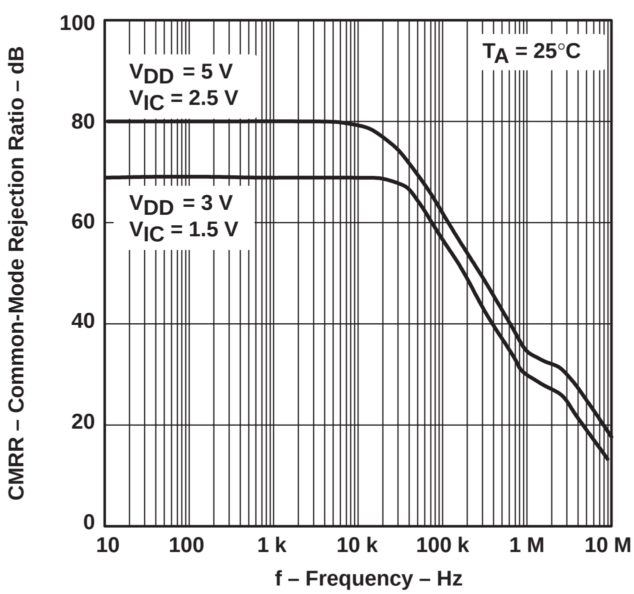


Figure 25

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

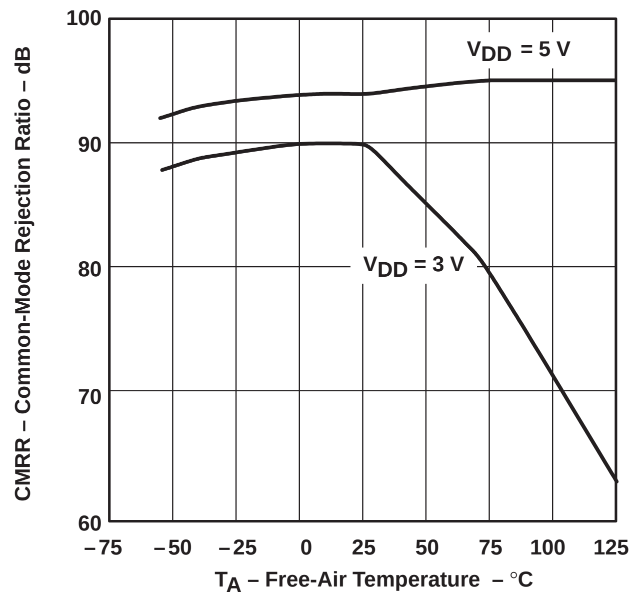


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

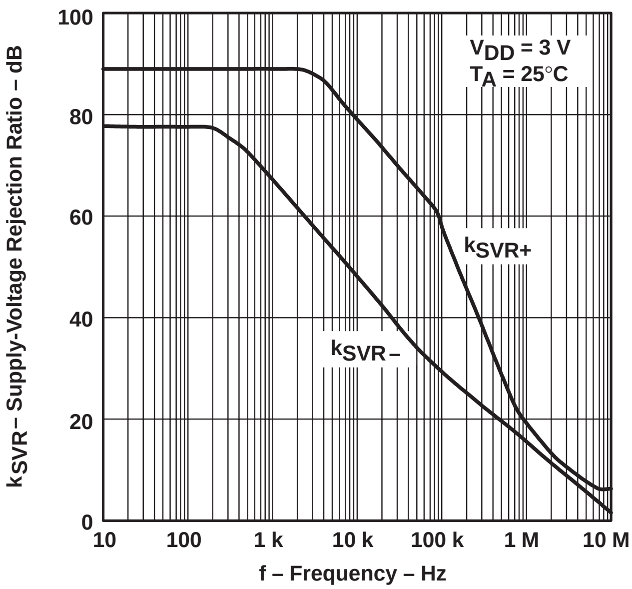


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

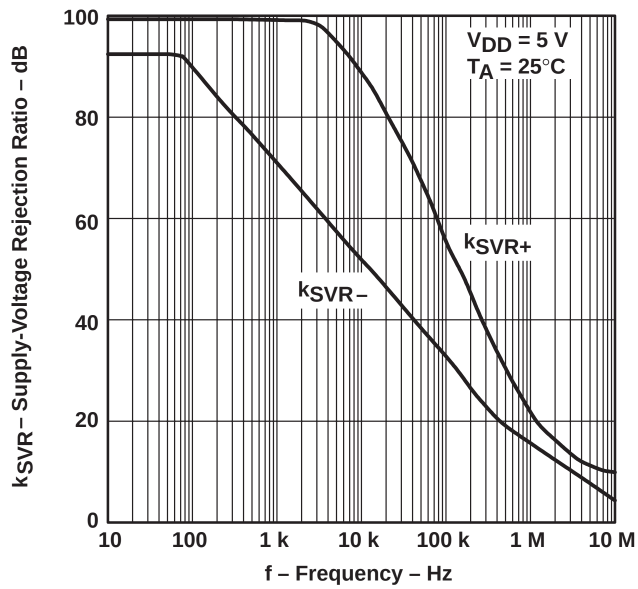


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

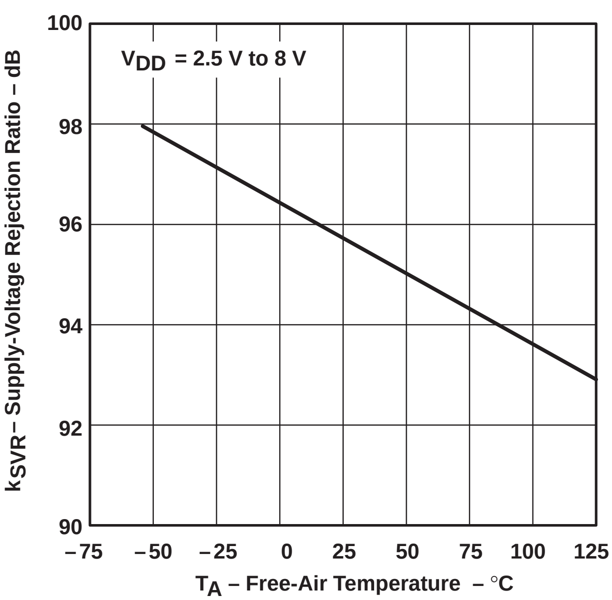


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

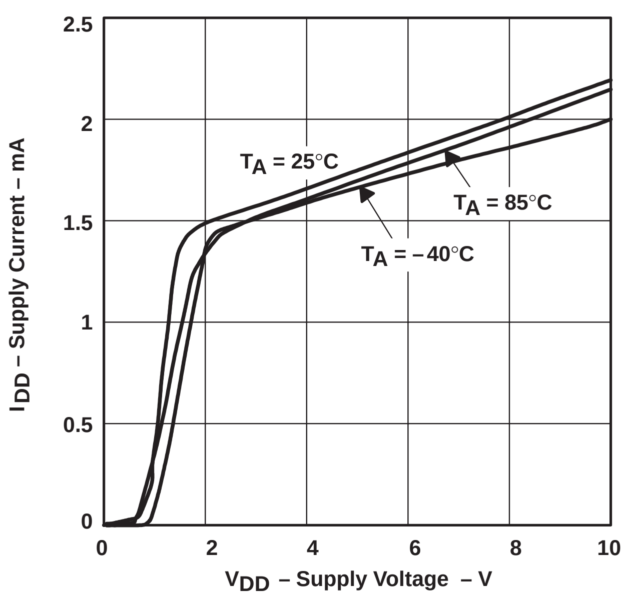


Figure 30

TYPICAL CHARACTERISTICS

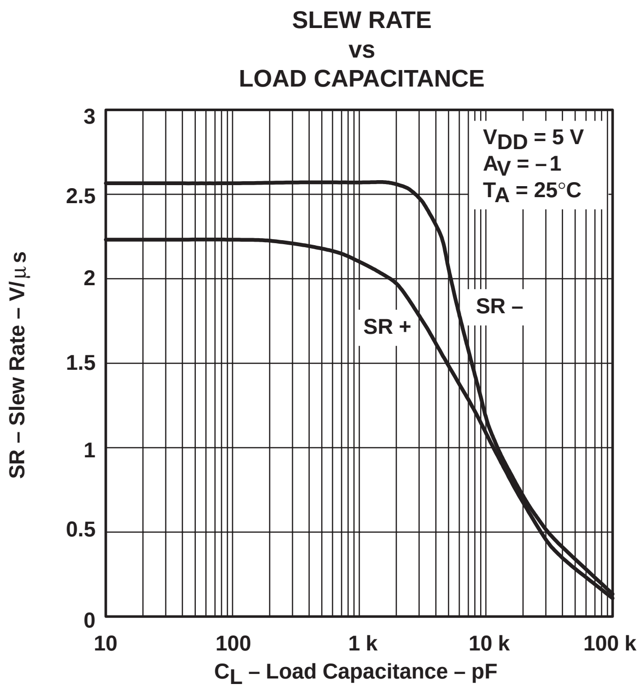


Figure 31

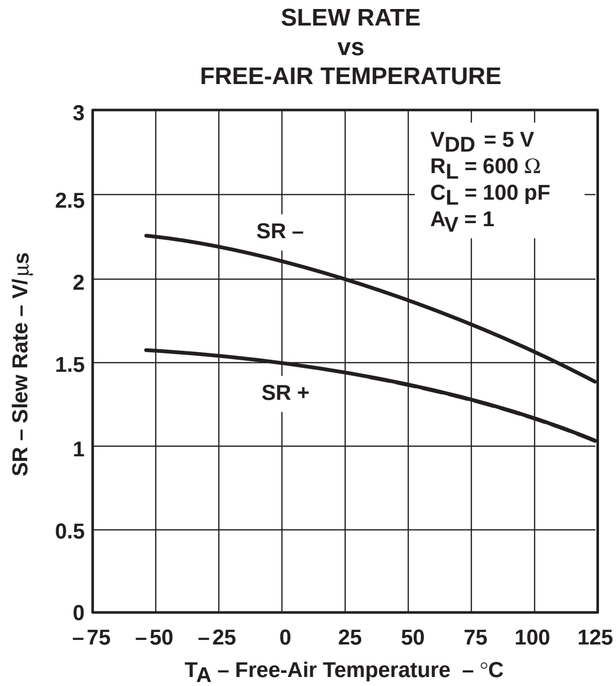
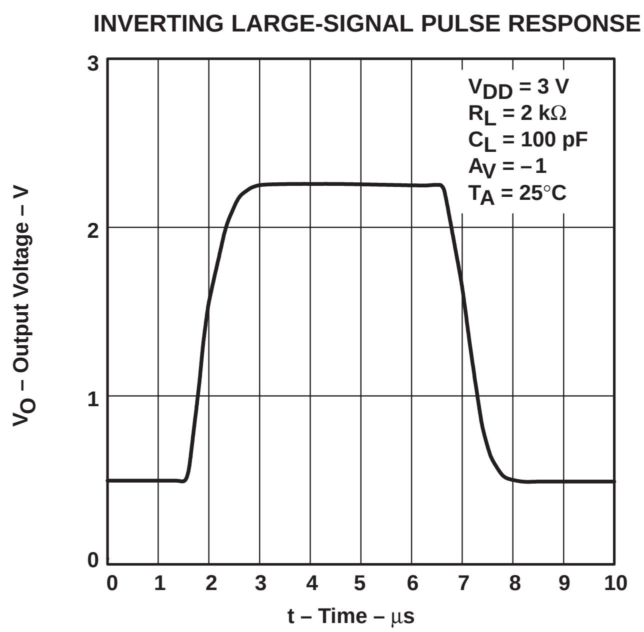


Figure 32



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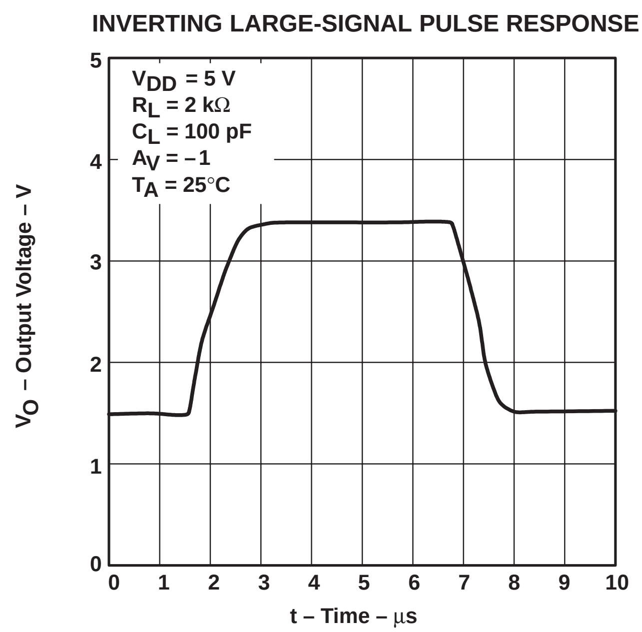
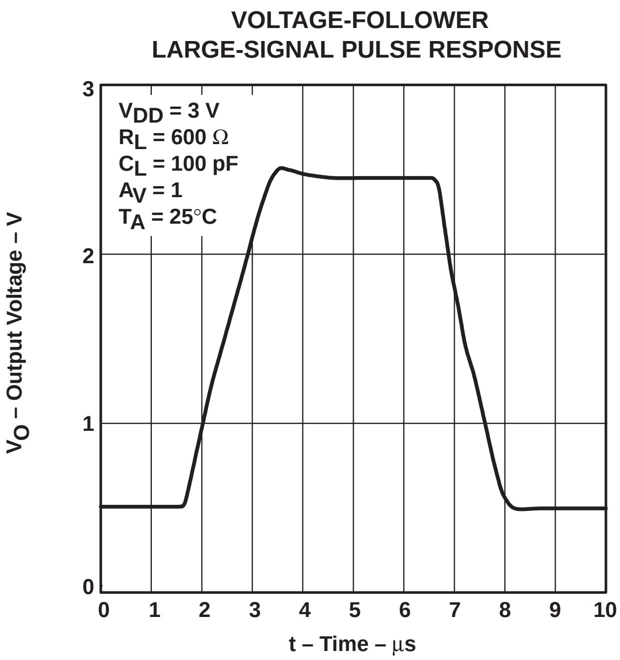


Figure 34

TYPICAL CHARACTERISTICS



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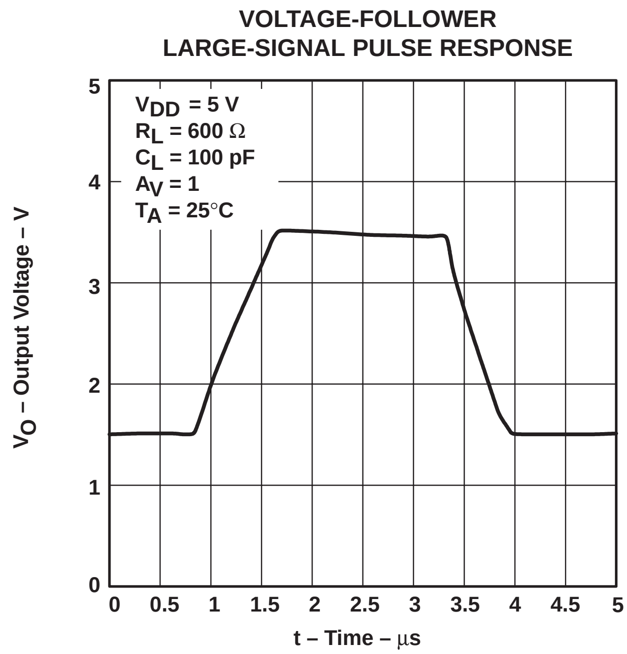

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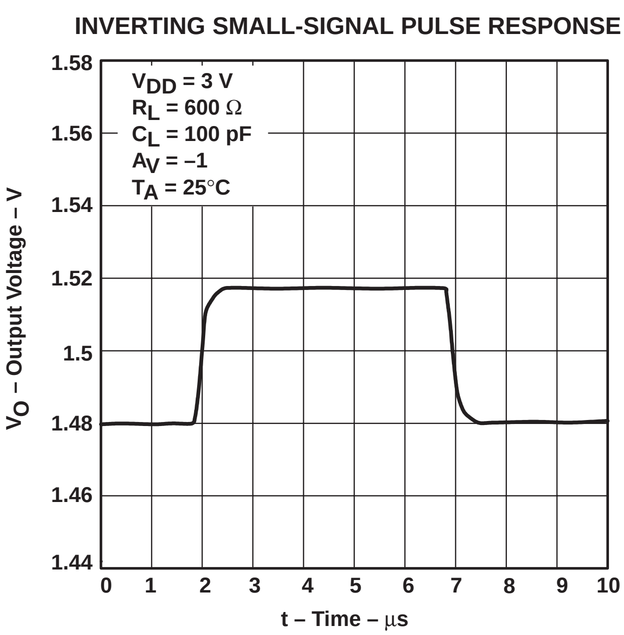


Figure 37

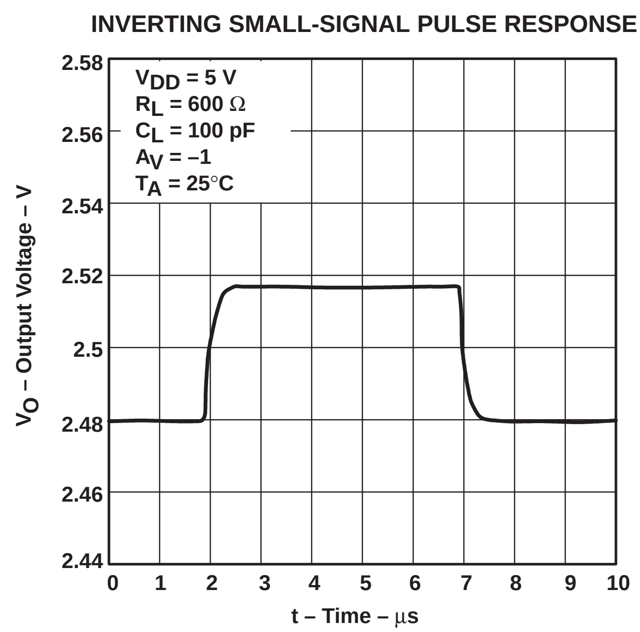


Figure 38

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

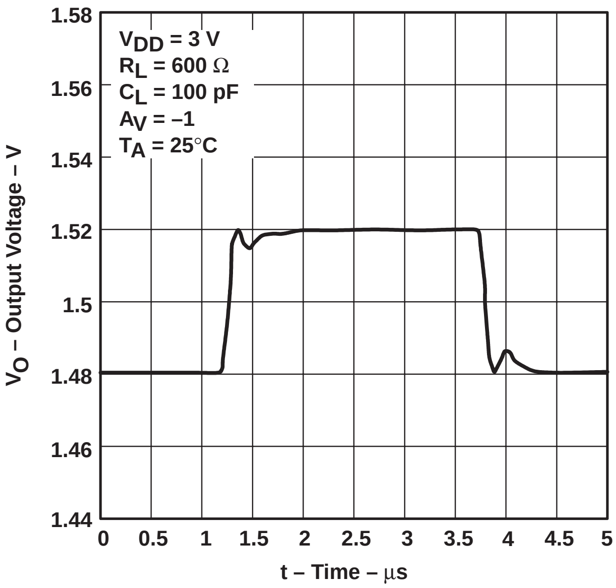


Figure 39

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

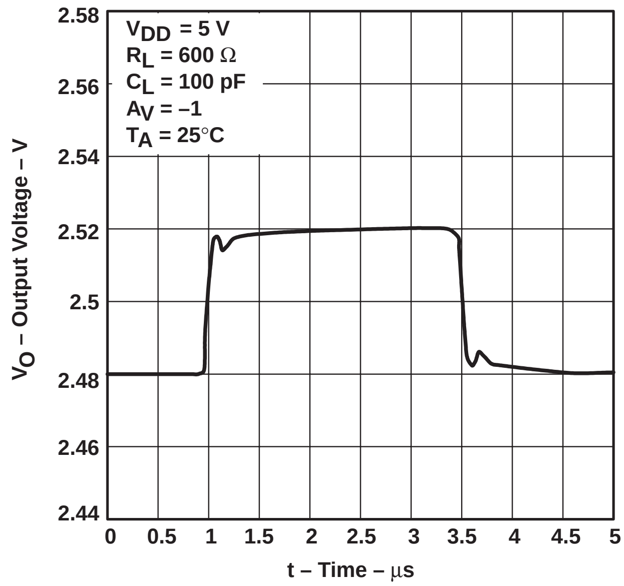


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

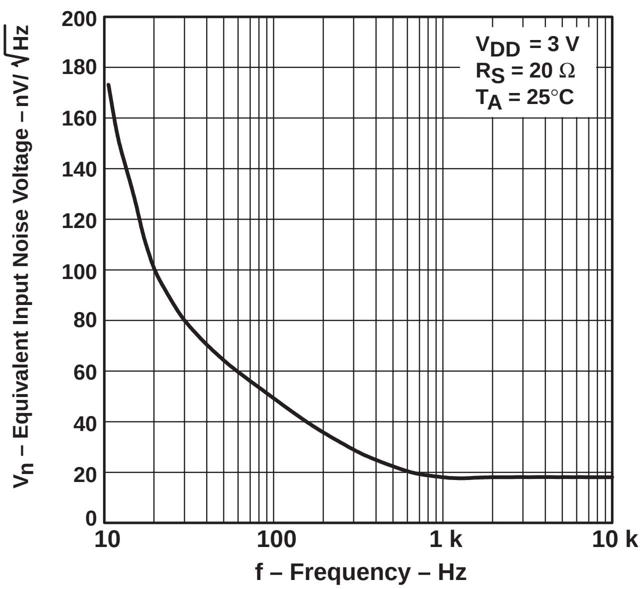


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

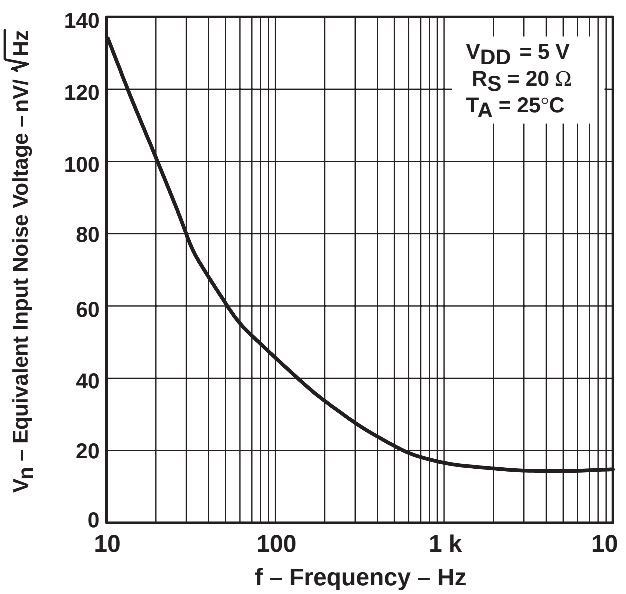


Figure 42

TYPICAL CHARACTERISTICS

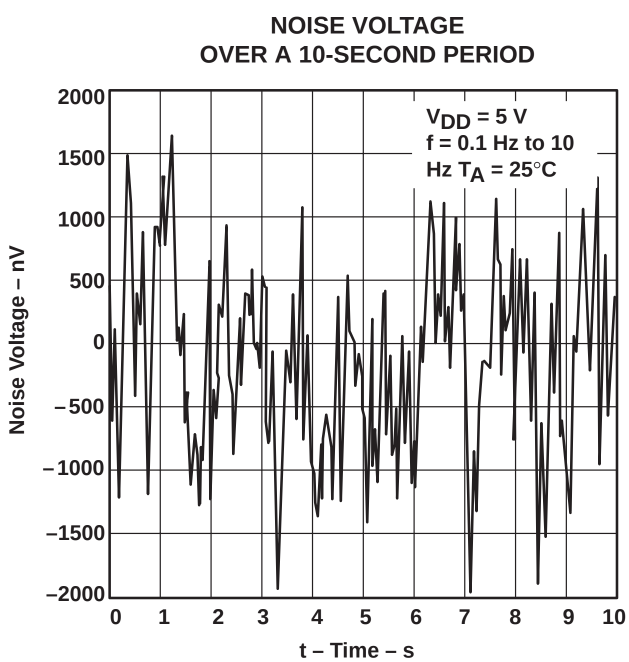


Figure 43

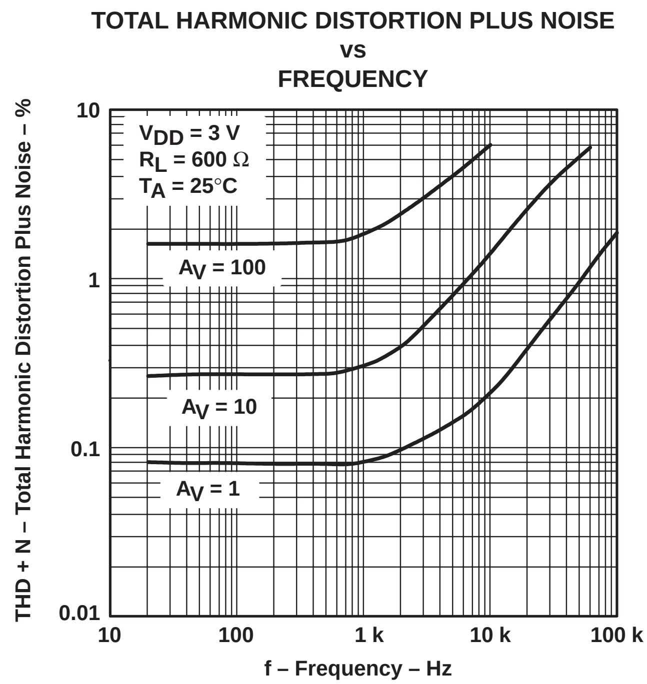


Figure 44

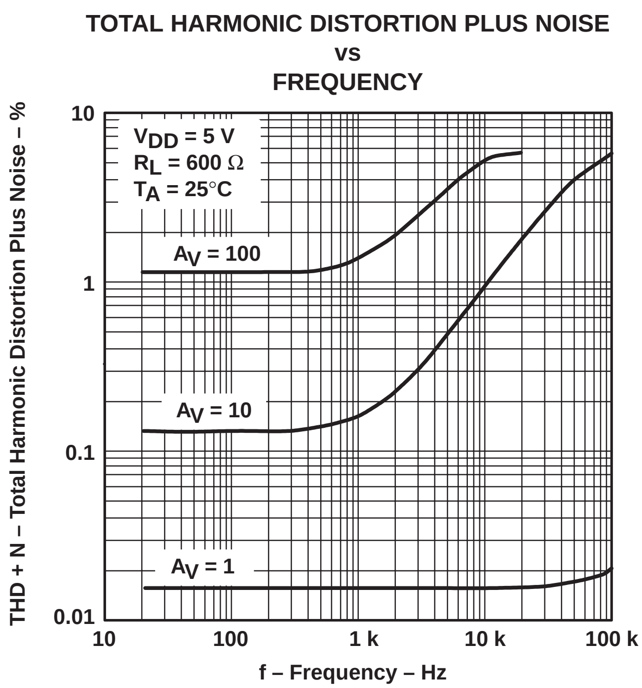


Figure 45

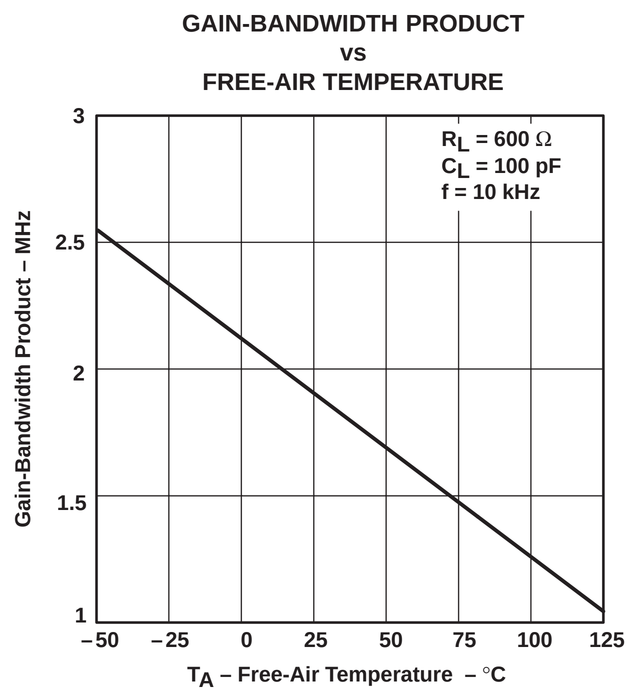


Figure 46

TYPICAL CHARACTERISTICS

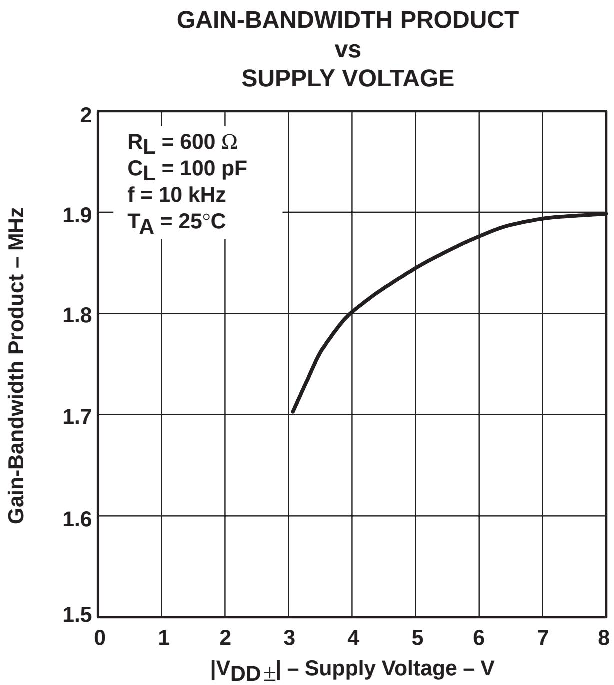


Figure 47

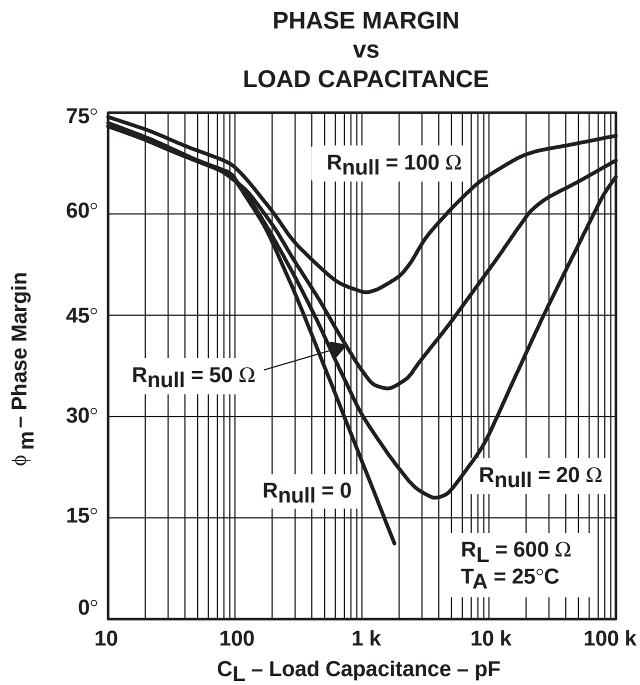


Figure 48

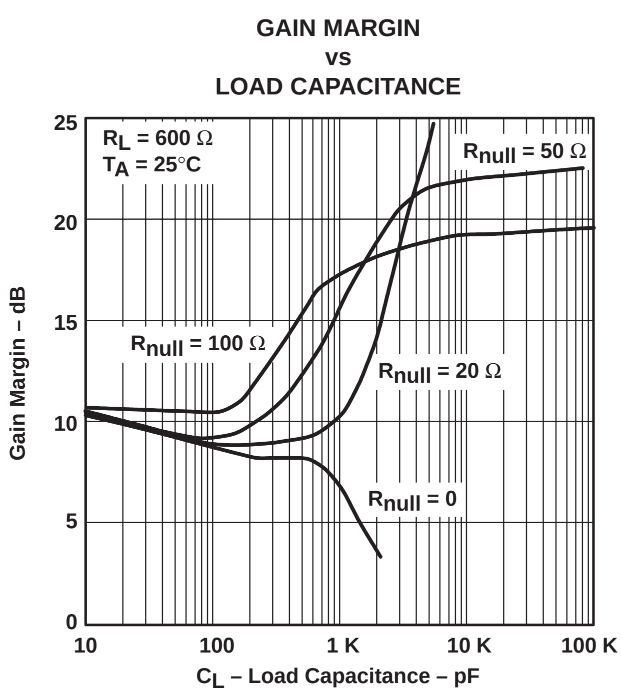


Figure 49

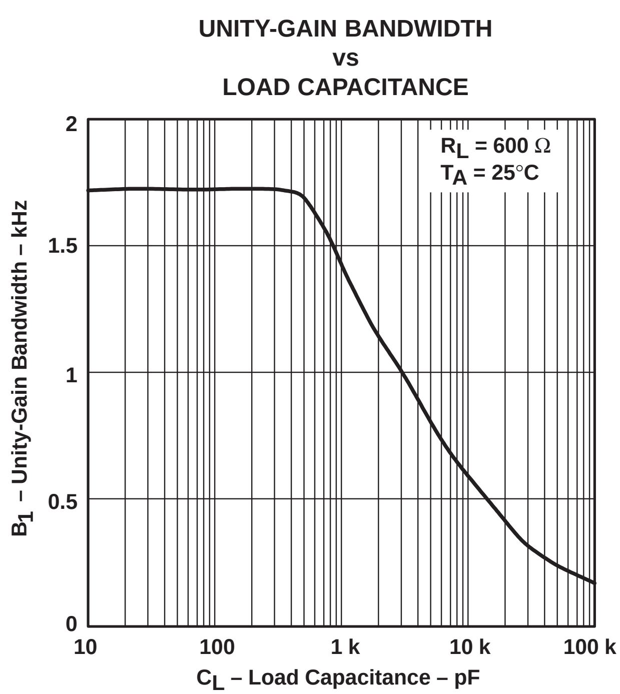


Figure 50

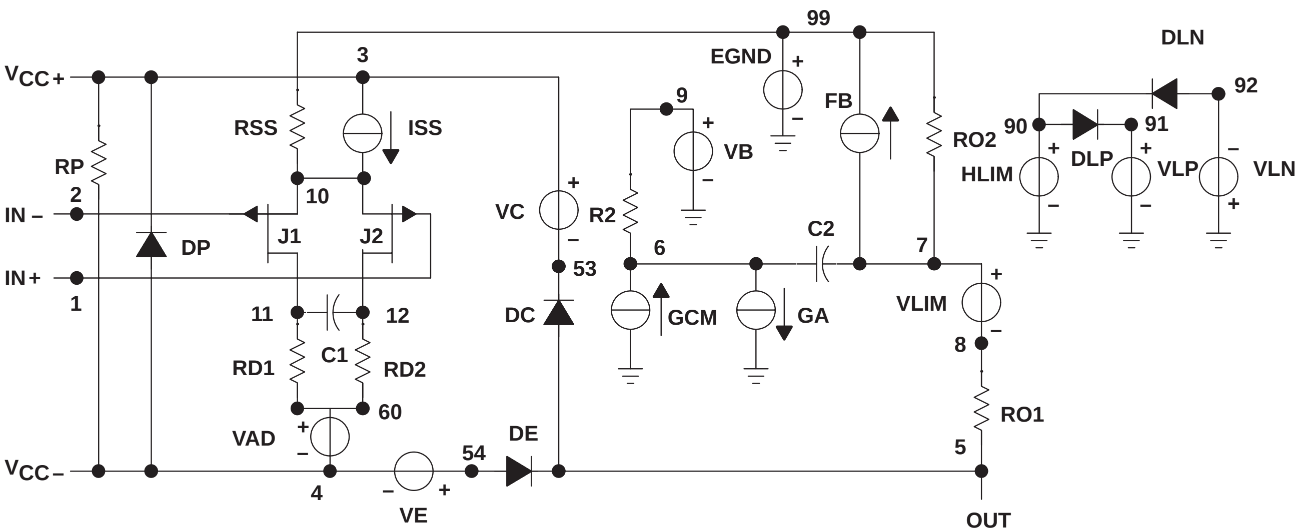
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 51 were generated using the TLV2442 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2442 1 2 3 4 5
C1     11     12     14E–12
C2     6      7      60.00E–12
DC     5      53     DX
DE     54     5      DX
DLP    90     91     DX
DLN    92     90     DX
DP     4      3      DX
EGND   99     0      POLY (2) (3,0) (4,) 0 .5 .5
FB     7      99     POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 –1E6 1E6 1E6 –1E6
GA     6      0      11     12 377.0E–6
GCM    0      6      10     99 134E–9
ISS    3      10     DC 216.OE–6
HLIM   90     0      VLIM 1K
J1     11     2      10 JX
J2     12     1      10 JX
R2     6      9      100.OE3
RD1    60     11     2.653E3
RD2    60     12     2.653E3
R01    8      5      50
R02    7      99     50
RP     3      4      4.310E3
RSS    10     99     925.9E3
VAD    60     4      –.5
VB     9      0      DC 0
VC     3      53     DC .78
VE     54     4      DC .78
VLIM   7      8      DC 0
VLP    91     0      DC 1.9
VLN    0      92     DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=1.500E–12BETA=1.316E-3
+ VTO=–.270)
.ENDS
```

Figure 51. Boyle Macromodel and Subcircuit

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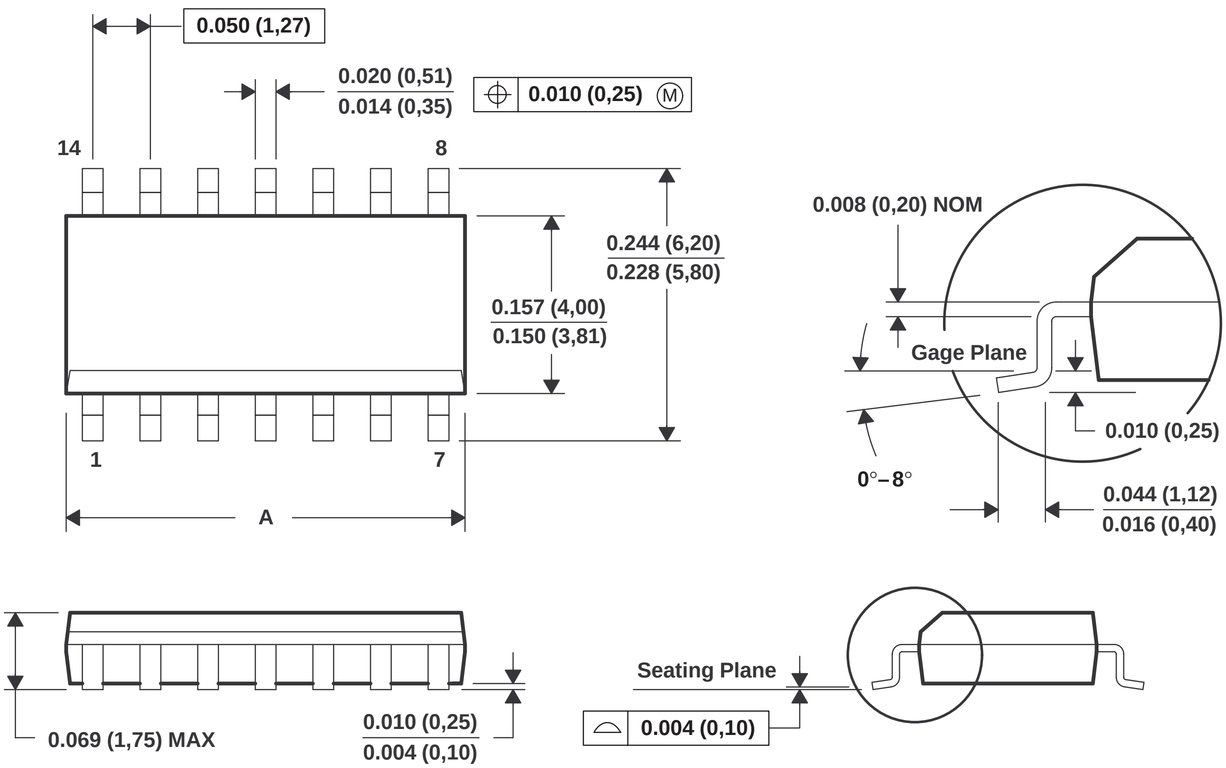
MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

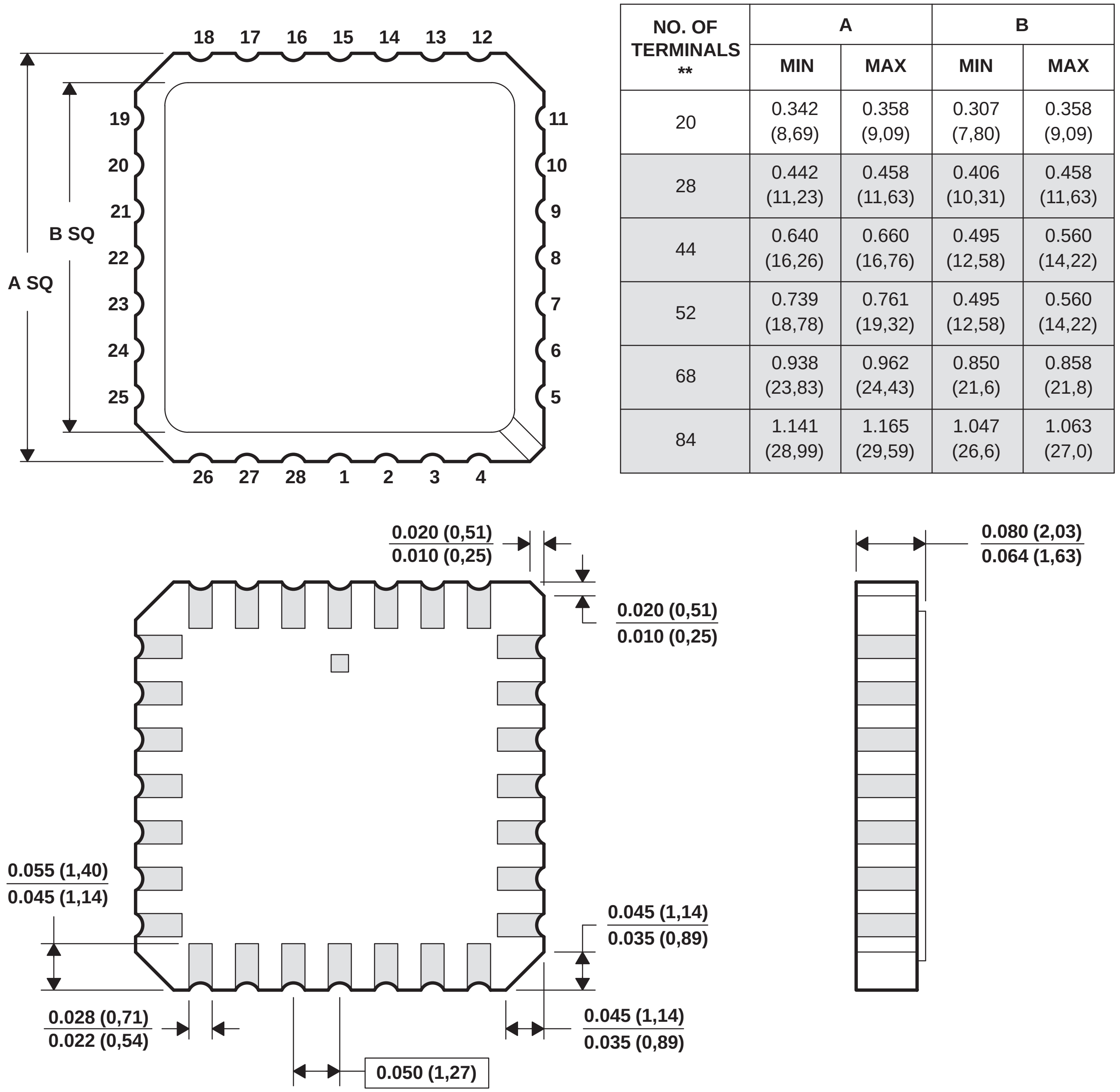
4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



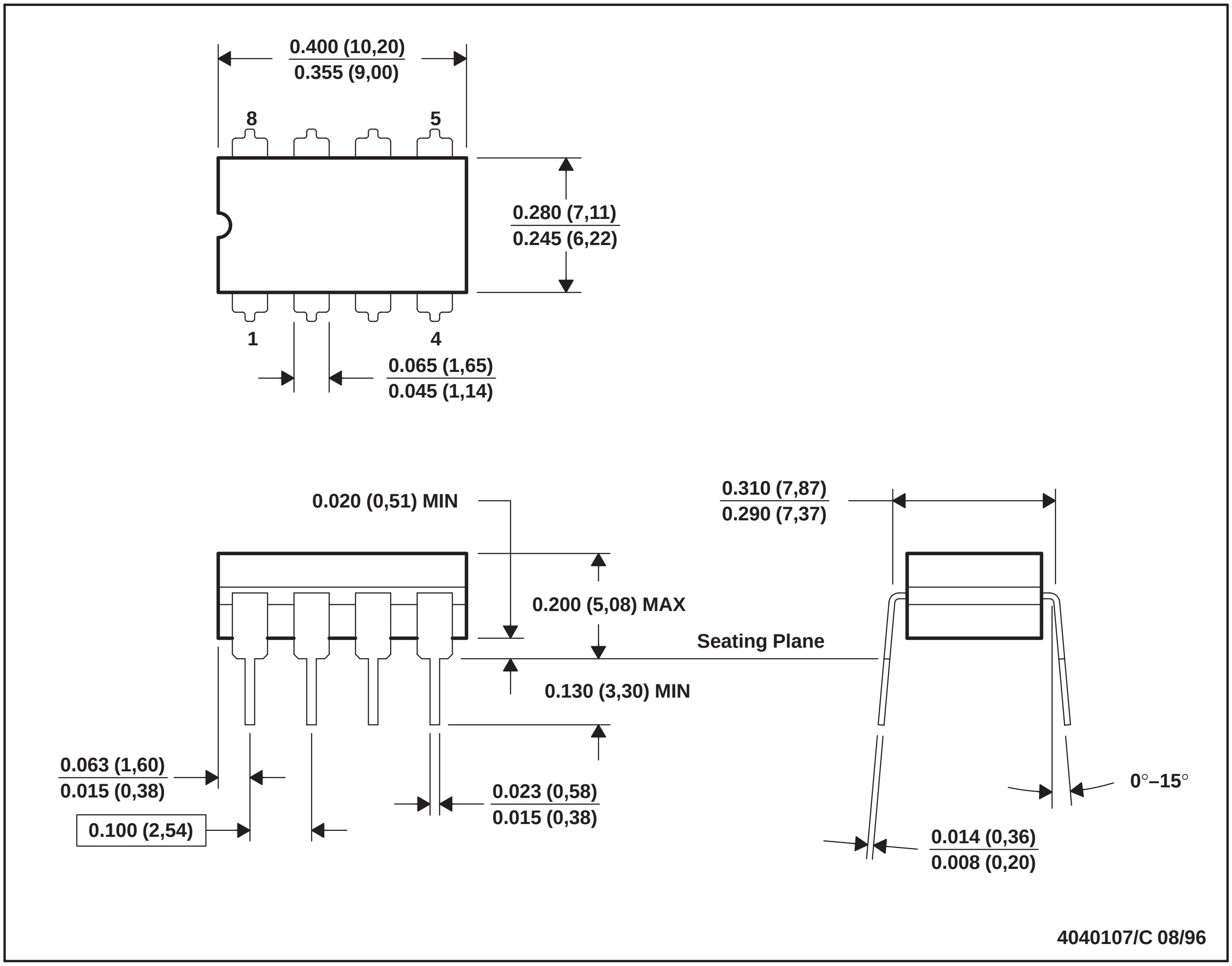
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**

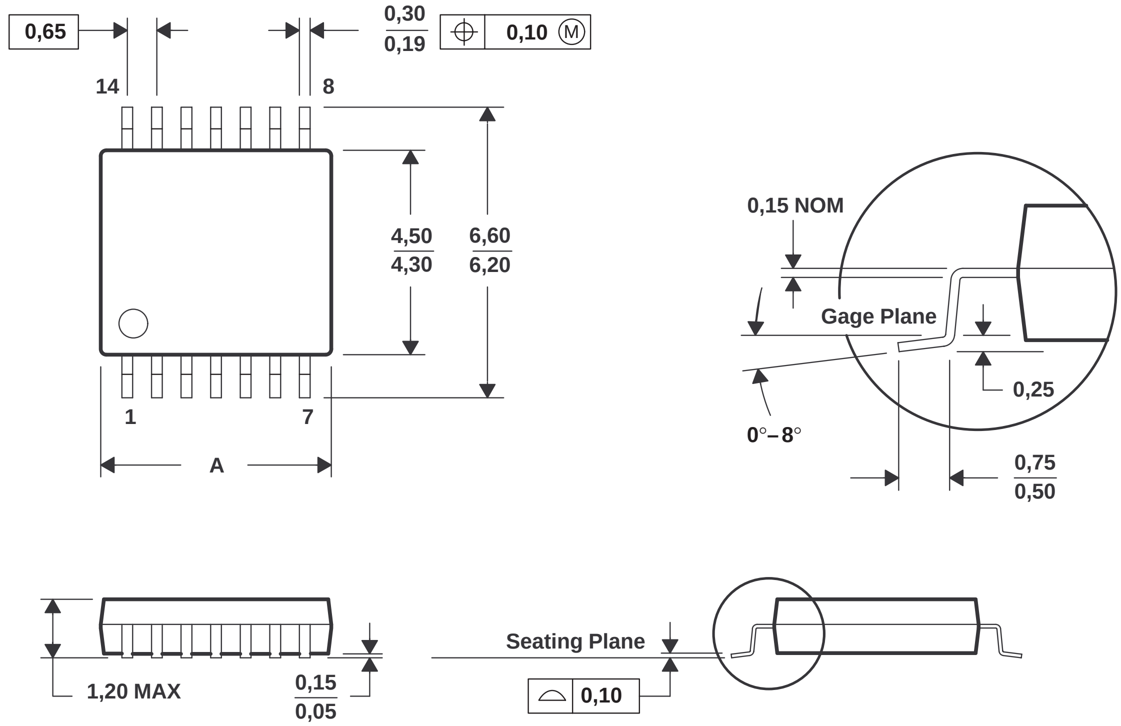


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



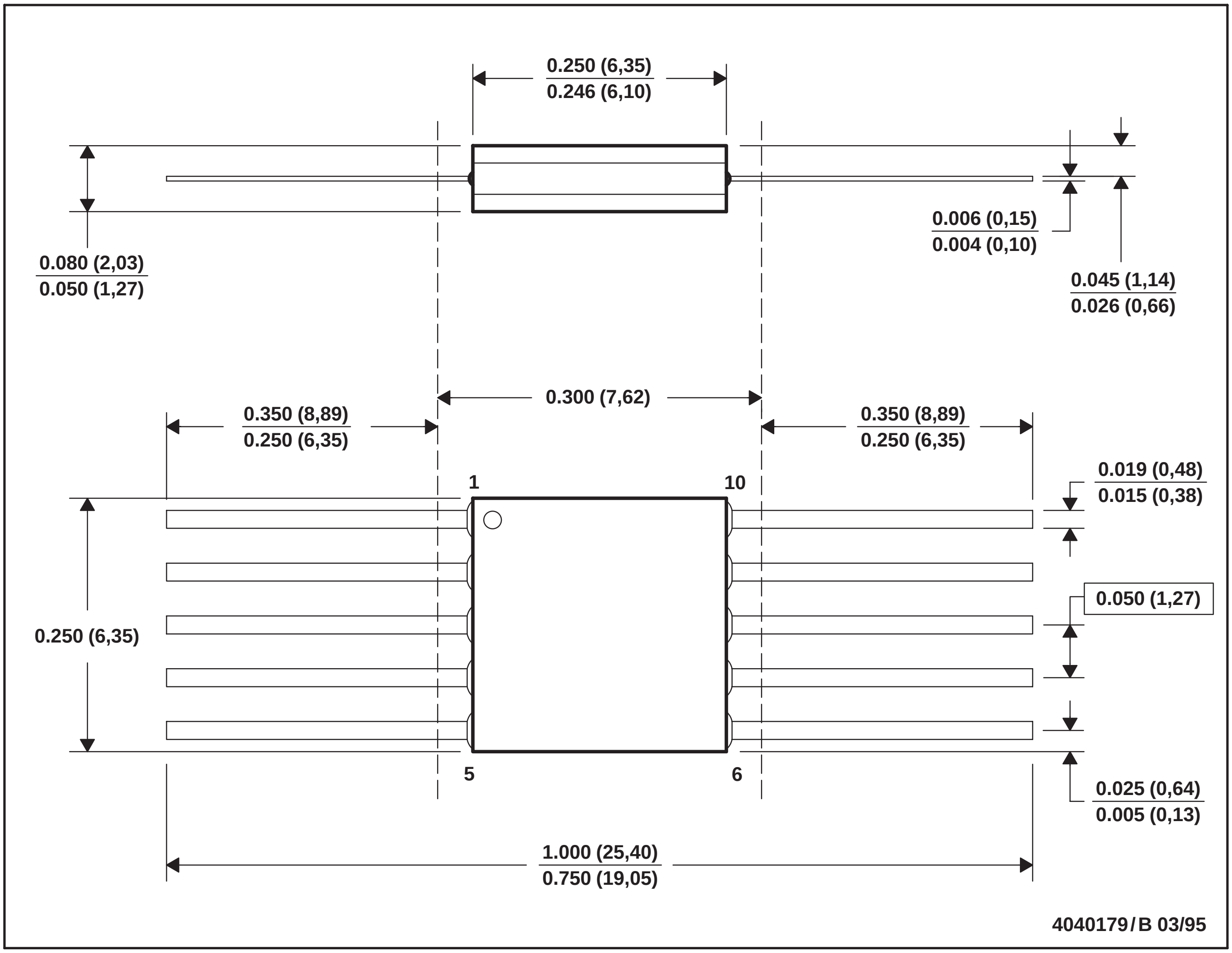
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064 / E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

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