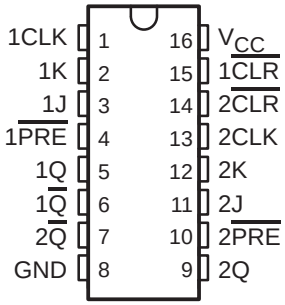
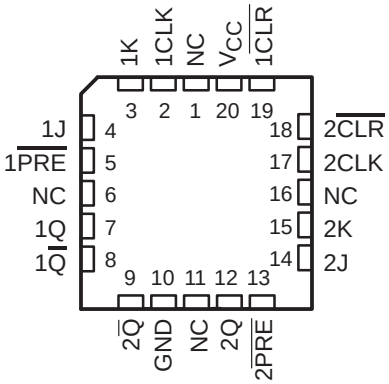
- **Fully Buffered to Offer Maximum Isolation From External Disturbance**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
′ALS112A	50	6

SN54ALS112A . . . J PACKAGE
SN74ALS112A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS112A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

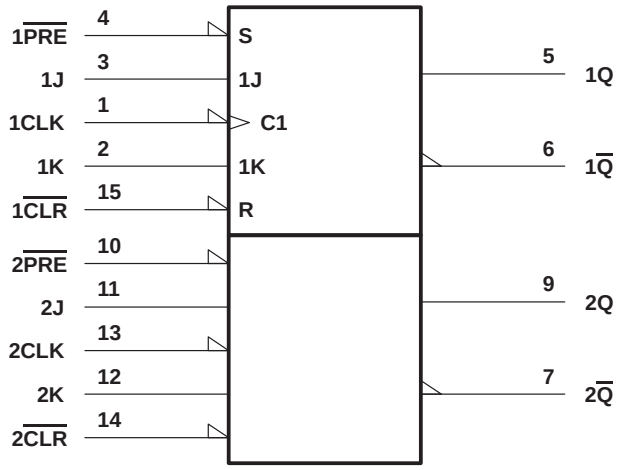
The SN54ALS112A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS112A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

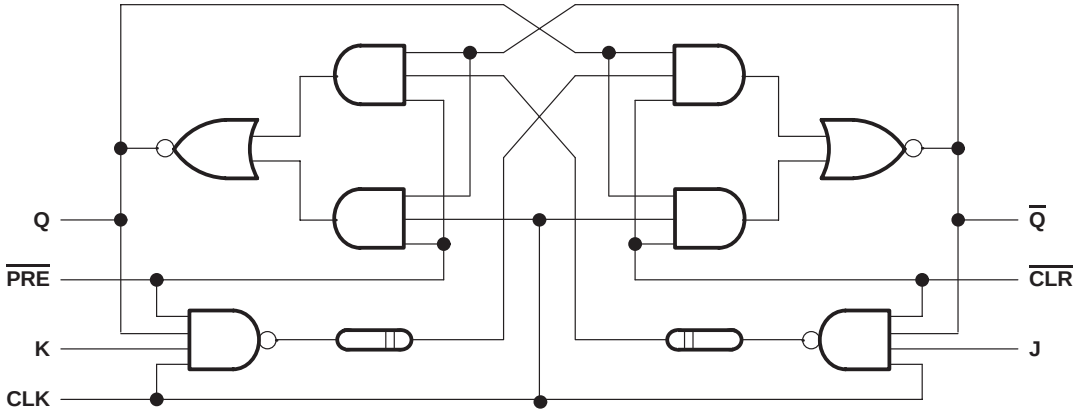
† The output levels in this configuration may not meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS112A . . . . . –55°C to 125°C
SN74ALS112A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				–0.4			–0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time after CLK↓	Data	0			0			ns
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					–0.4			–0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

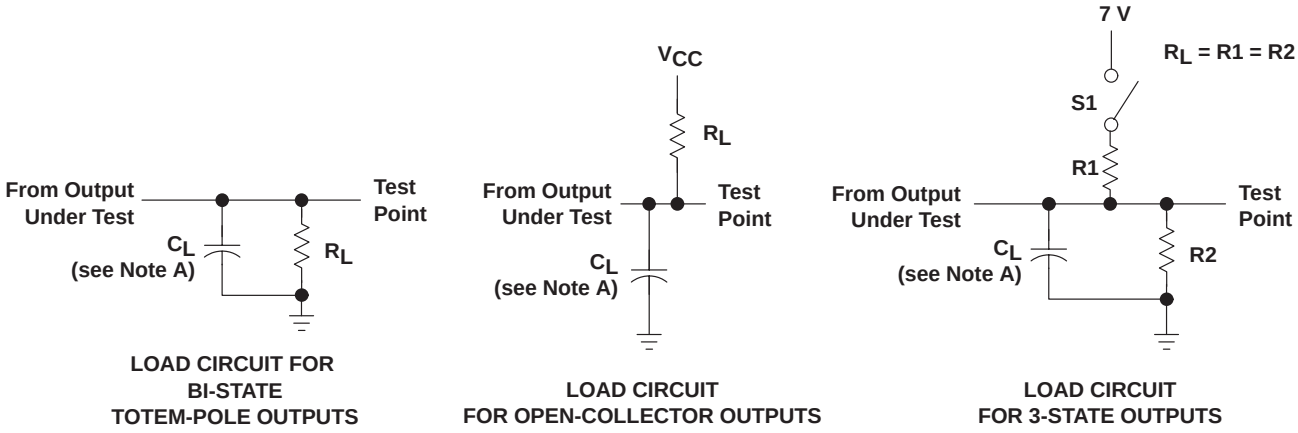
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	26	3	15	ns
t_{PHL}			4	23	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	23	3	15	ns
t_{PHL}			5	24	5	19	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

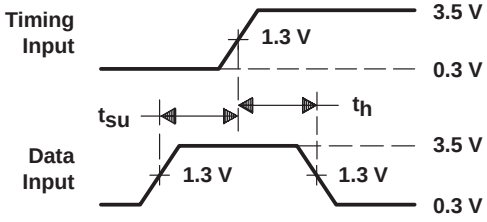
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



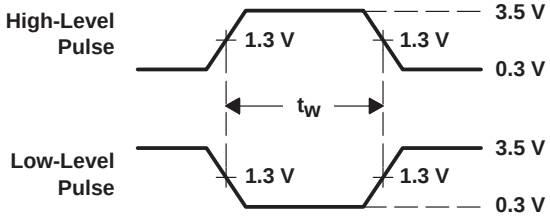
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

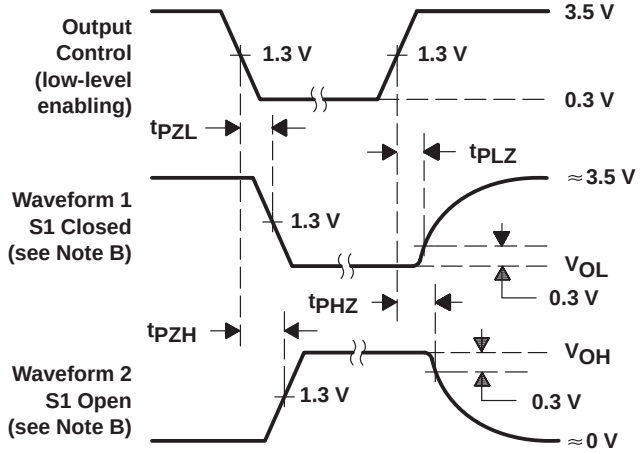
LOAD CIRCUIT FOR 3-STATE OUTPUTS



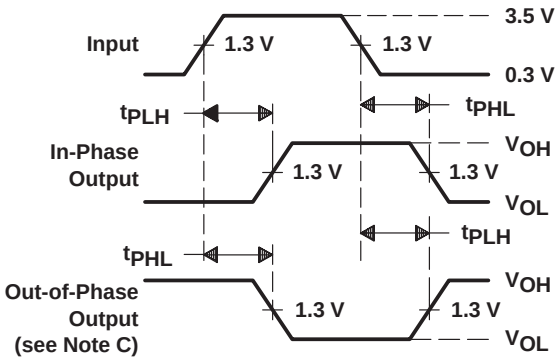
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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SN74ALS112A, Dual J-K Negative-Edge-Triggered Flip-Flops With Clear and Preset

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS112A	SN74ALS112A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	2	2
th (ns)		0
tpd max (ns)		19
tsu (ns)		22

FEATURES

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- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

DESCRIPTION

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These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74als112a.pdf (96 KB,Rev.A) (Updated: 12/01/1994)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74ALS112AD	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.35	40	N/A*	400 | 19 Sep	5 WKS	Avnet | AMERICA	>1k	BUY NOW
								469 | 03 Oct				
								>10k | 10 Oct				
								>10k | 17 Oct				
								>10k | 24 Oct				
SN74ALS112ADR	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.38	2500	N/A*	469 | 03 Oct	5 WKS			
								>10k | 10 Oct				
								>10k | 17 Oct				
								>10k | 24 Oct				
								>10k | 31 Oct				
SN74ALS112AN	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.35	25	N/A*	469 | 02 Oct	5 WKS	Avnet | AMERICA	50	BUY NOW
								>10k | 07 Oct				

								>10k | 09 Oct						
								>10k | 16 Oct						
SN74ALS112AN3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available				
SN74ALS112ANSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.35	2000	N/A*	1641 | 23 Sep	5 WKS					
								2000 | 03 Oct						
								>10k | 04 Oct						
								2314 | 11 Oct						
								>10k | 18 Oct						

Table Data Updated on: 9/26/2002