MC74VHC393

Dual 4-Bit Binary Ripple Counter

The MC74VHC393 is an advanced high speed CMOS dual 4–bit binary ripple counter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of two independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷256 counter can be obtained by cascading the two binary counters.

Internal flip–flops are triggered by high–to–low transitions of the clock input. Reset for the counters is asynchronous and active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the VHC393.

The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

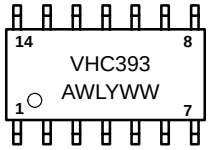
- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 236 FETs or 59 Equivalent Gates

ON Semiconductor

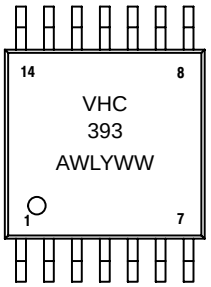
http://onsemi.com

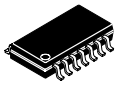
MARKING DIAGRAMS

SOIC–14
D SUFFIX
CASE 751A

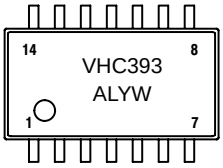


TSSOP–14
DT SUFFIX
CASE 948G





SOIC EIAJ–14
M SUFFIX
CASE 965



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC393D	SOIC–14	55 Units/Rail
MC74VHC393DR2	SOIC–14	1000 Units/Reel
MC74VHC393DT	TSSOP–14	96 Units/Rail
MC74VHC393DTR2	TSSOP–14	2500 Units/Reel
MC74VHC393M	SOIC EIAJ–14	50 Units/Rail
MC74VHC393MEL	SOIC EIAJ–14	2000 Units/Reel

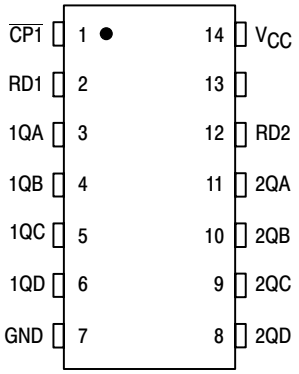


Figure 1. Pin Assignment

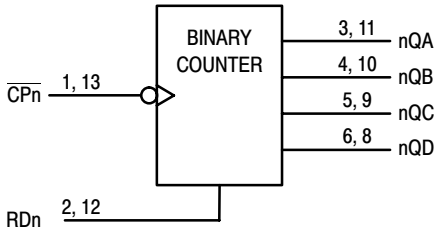


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs		
Clock	**Reset**	**Outputs**
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Next State

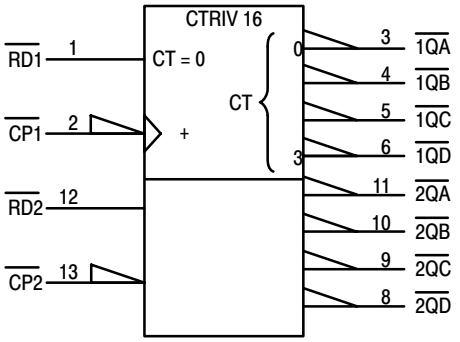


Figure 3. IEC Logic Symbol

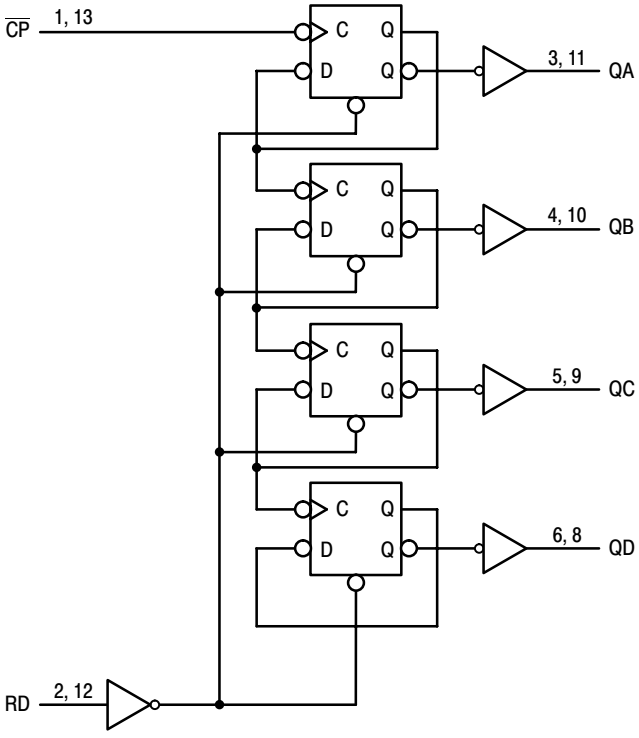


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage	– 0.5 to + 7.0	V
V_{OUT}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V	0	100	ns/V
		V_{CC} = 5.0V	0	20	

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

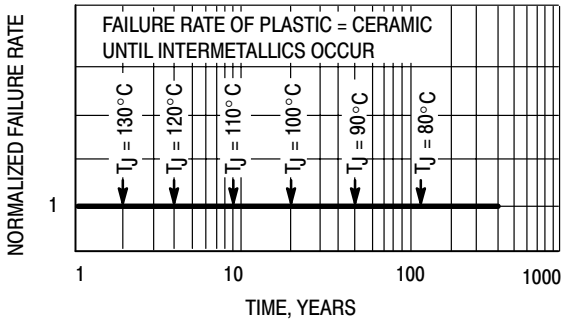


Figure 5. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = – 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = –4 mA I_{OH} = –8 mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF	75 45	120 65		65 35		65 35		MHz
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF	125 85	170 115		105 75		105 75		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QA	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		8.6 11.1	13.2 16.7	1.0 1.0	15.5 19.0	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		5.8 7.3	8.5 10.5	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QB	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		10.2 12.7	15.8 19.3	1.0 1.0	18.5 22.0	1.0 1.0	18.5 22.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		6.8 8.3	9.8 11.8	1.0 1.0	11.5 13.5	1.0 1.0	11.5 13.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QC	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		11.7 14.2	18.0 21.5	1.0 1.0	21.0 24.5	1.0 1.0	21.0 24.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		7.7 9.2	11.2 13.2	1.0 1.0	13.0 15.0	1.0 1.0	13.0 15.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QD	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		13.0 15.5	19.7 23.2	1.0 1.0	23.0 26.5	1.0 1.0	23.0 26.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		8.5 10.0	12.5 14.5	1.0 1.0	14.5 16.5	1.0 1.0	14.5 16.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = \leq 85°C$		$T_A = \leq 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Maximum Propagation Delay, RD to QN	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$pF		7.9	12.3	1.0	14.5	1.0	14.5	ns
		$C_L = 50$pF		10.4	15.8	1.0	18.0	1.0	18.0	
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$pF		5.4	8.1	1.0	9.5	1.0	9.5	ns
		$C_L = 50$pF		6.9	10.1	1.0	11.5	1.0	11.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$pF (Note 1.)			1.5		1.5		1.5	pF
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$pF (Note 1.)			1.0		1.0		1.0	pF
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	23	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.5	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = \leq 85°C$	$T_A = \leq 125°C$	Unit
			Typ	Limit	Limit	Limit	
t_w	Minimum Pulse Width, $\overline{CP}$	$V_{CC} = 3.3 \pm 0.3$ V		5.0	5.0	5.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V		5.0	5.0	5.0	
t_w	Minimum Pulse Width, RD	$V_{CC} = 3.3 \pm 0.3$ V		5.0	5.0	5.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V		5.0	5.0	5.0	
t_{rec}	Minimum Recovery Time, RD to $\overline{CP}$	$V_{CC} = 3.3 \pm 0.3$ V		5.0	5.0	5.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V		4.0	4.0	4.0	
t_r, t_f	Minimum Input Rise and Fall Times	$V_{CC} = 3.3 \pm 0.3$ V		330	330	330	ns
		$V_{CC} = 5.0 \pm 0.5$ V		100	100	100	

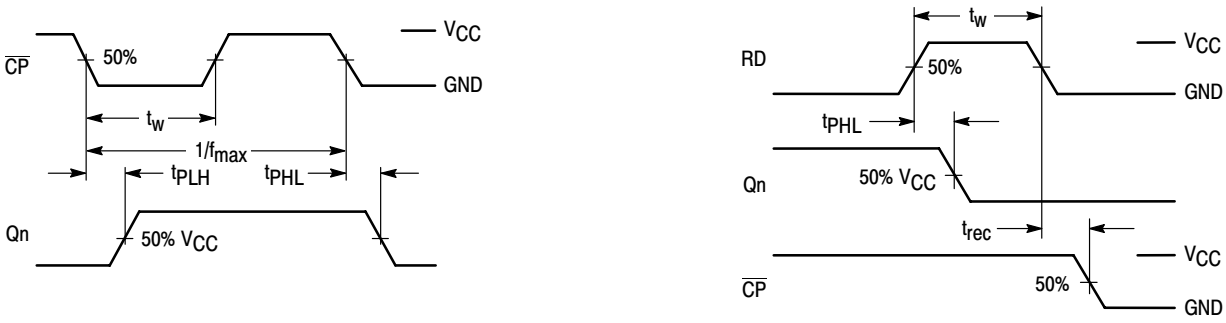
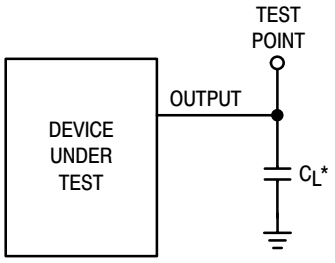


Figure 6. Switching Waveforms



*Includes all probe and jig capacitance

Figure 7. Test Circuit

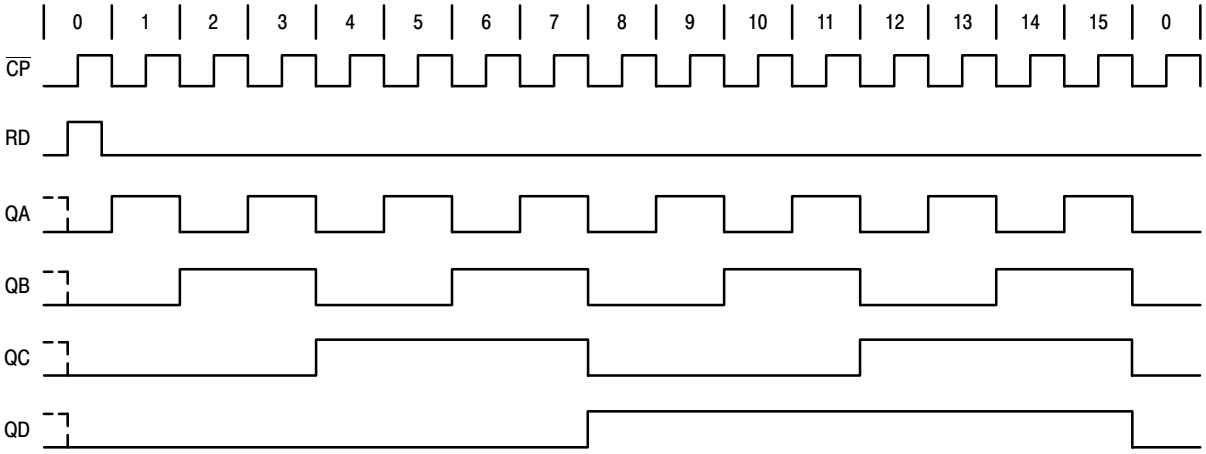


Figure 8. Timing Diagram

COUNT SEQUENCE

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H