CMOS MD4332B
32 Segment LCD Driver

Feb. 1985

Features

- CMOS Low power.
- 3 to 18 volt operation.
- On-chip wave-shaping.
- High-speed (typ. 3 MHz) shift register.

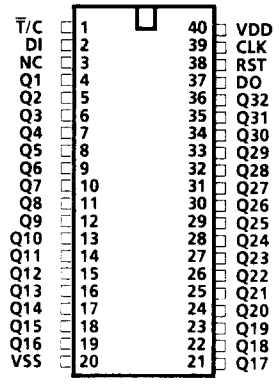
Applications

- Telephone displays.
- Instrumentation readouts.
- Microprocessor displays.
- Digital clock, counter.

Description

The MD4332B is a CMOS 32-bit static shift register incorporating selectable true/complement outputs for each bit. This device is well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. The device can drive four 7-segment displays or two 14-segment alphanumeric displays plus decimal points or two 16-segment alphanumeric displays directly.

Pin Connections



Ordering Information -40° to 85°C

MD4332BC	40 Pin Ceramic DIP
MD4332BE	40 Pin Plastic DIP

5

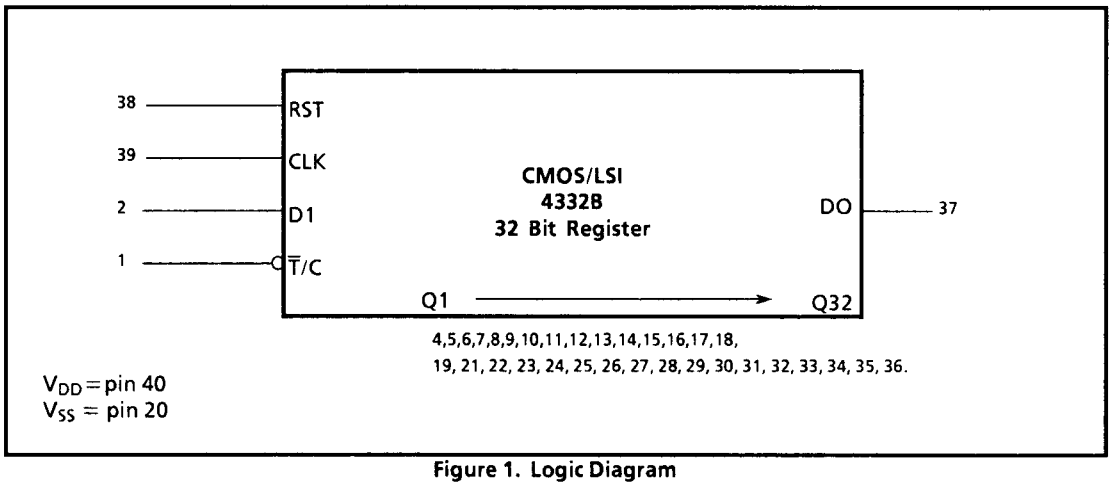


Figure 1. Logic Diagram

Absolute Maximum Ratings*- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	DC Supply Voltage		V_{DD}	-0.5	18	V
2	Input Voltage		V_{IN}	-0.5	V_{DD} + 0.5	V
3	DC Current Drain per Pin		I		±10	mA
4	Storage Temperature		T_{STG}	-65	+125	°C
5	Power Dissipation	Plastic	P_D		0.6	W
		Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1		Supply Voltage	V_{DD}	3	5	18	V	
2		Input Voltage	V_I	0		V_{DD}	V	
3		Output Voltage	V_O	0		V_{DD}	V	
4		Operating Temperature	T_A	-40	25	85	°C	

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	INPUTS	Quiescent Device Current	I_L		0.5	50	µA	V_{DD} = 5V
			I_L		1	100	µA	V_{DD} = 10V
2		Input Current	I_Z		10		pA	
3		Noise Immunity (Any Input)	V_{NL}	1.5	2.25		V	V_{DD} = 5V, V_{OUT} = 0.8V
			V_{NH}	3	4.5		V	V_{DD}= 10V, V_{OUT} = 1.0V
4		Noise Immunity (Any Input)	V_{NH}	1.5	2.25		V	V_{DD} = 5V, V_{OUT} = 4.2V
			V_{NH}	3	4.5		V	V_{DD} = 10V, V_{OUT} = 9.0V
5	OUTPUTS	Output Low Voltage	V_{OL}		0	0.01	V	V_{DD}= 5V
			V_{OL}		0	0.01	V	V_{DD} = 10V
6		Output High Voltage	V_{OH}	4.99	5		V	V_{DD}= 5V
			V_{OH}	9.99	10		V	V_{DD} = 10V
7		Output Drive Current D_{OUT} N-Channel	I_{DN}	0.8	1.7		mA	V_{OUT}=0.5V, V_{DD}=5V
			I_{DN}	1.0	3.0		mA	V_{OUT}=0.5V, V_{DD}=10V
8		Output Drive Current D_{OUT} P-Channel	I_{DP}	0.35	-0.9		mA	V_{OUT}=4.5V, V_{DD}=5V
			I_{DP}	-0.8	-1.9		mA	V_{OUT}=9.5V, V_{DD}=10V
9		Output Drive Current Q_{OUT} N-Channel	I_{DN}	50	250		µA	V_{OUT}=0.5V, V_{DD}=10V
		P-Channel	I_{DP}	-50	-250		µA	V_{OUT}=9.5V, V_{DD}=10V

† T_A = 25°C

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Propagation Delay Time	t_{PHL} t_{PLH}		300 300		ns ns	V_{DD} = 10V V_{DD} = 10V
2	Transition Time	t_{THL} t_{TLH}		70 300	130	ns ns	V_{DD} = 10V, DO (C_L = 50pF) V_{DD} = 10V, Q1-Q32 (C_L = 15pF)
3	Maximum Clock Frequency	f_{CL}	1.0	3.0		MHz	V_{DD} = 10V
4	Minimum Clock Pulse Width	t_{WL} t_{WH}		200 200		ns ns	V_{DD} = 10V V_{DD} = 10V
5	Minimum Reset Pulse Width	$t_{WH(R)}$		200		ns	V_{DD} = 10V
6	Input Capacitance	C_I		5		pF	Any Input

† T_A = 25°C, C_L = 50 pF. Typical temperature coefficient for all values of V_{DD} = 0.3% per °C. All input rise and fall times = 20ns.

Pin Description

Pin #	Name	Description
1	$\overline{T}$/C	**True/Complement Input.** This is the control input to select the form of logic (True/complementary) used by the outputs (Q1-Q32).
2	DI	**Serial Data Input.** This is the serial data input of the internal shift register.
3	NC	**No Connection.**
4-19	Q1-Q16	**True/Complement Outputs.** These are the parallel outputs of the internal 32-bit shift register.
20	V_{SS}	**Ground 0V.**
21-36	Q17-Q32	**True/Complement Outputs.** These are the parallel outputs of the internal 32-bit shift register.
37	DO	**Serial Data Output.** This can be connected to the DI input of another MD4332B to form longer shift register.
38	RST	**Master Reset Input.** A logic high on this input resets the device.
39	CLK	**Clock Input.** The clock input is positive edge-triggered.
40	VDD	**Positive Power Supply.** 3V-18V operation.

5

Functional Description

The MD4332B is a CMOS/LSI static shift register designed to drive all types of LCD readouts directly or as serial-to-parallel converter where both the true and complementary parallel outputs are available.

The circuit accepts a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of this circuit is that the clock input and the true/complement control ($\overline{T}$/C) input have wave-shaping circuits to ensure fast edges on-chip regardless of the shape of the incoming signals.

The 4332B has asynchronous reset (RST) inputs which are active logic-level HIGH.

The parallel outputs of the shift register are available in either true or complementary form dependent on the state of the true-complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in the register. This action is independent of the clock input condition. A serial data (DO) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

Application