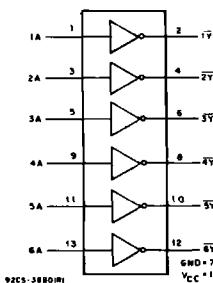


CD54/74AC04, CD54/74AC05

CD54/74ACT04, CD54/74ACT05



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The RCA-CD54/74AC04, -05 and CD54/74ACT04, -05 hex inverters use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT04 have active outputs; the CD54/74AC/ACT05 have open-drain outputs.

The CD74AC04, -05 and CD74ACT04, -05 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC04, -05 and CD54ACT04, -05, available in chip form (H suffix), are operable over the -55 to +125°C temperature.

TRUTH TABLES

CD54/74AC/ACT04

CD54/74AC/ACT05

INPUT	OUTPUT
A	Y
L	H
H	L

Z = High Impedance

INPUT	OUTPUT
A	Y
L	Z
H	L

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{cc})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{ix} (for $V_I < -0.5$ V or $V_I > V_{cc} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{ox} (for $V_O < -0.5$ V or $V_O > V_{cc} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_O > -0.5$ V or $V_O < V_{cc} + 0.5$ V)	± 50 mA*
DC V_{cc} or GROUND CURRENT (I_{cc} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to +100°C (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to +125°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For $T_A = -55$ to +70°C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	-55 to +125°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	+300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

Hex Inverters

CD54/74AC/ACT04 - Active Outputs

CD54/74AC/ACT05 - Open-Drain Outputs

Type Features:

- Buffered inputs
- Typical propagation delay (AC04/05):
3.5 ns @ $V_{cc} = 5$ V, $T_A = 25^\circ$ C, $C_L = 50$ pF

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24 -mA output drive current
 - Fanout to 15 FAST® ICs
 - Drives 50-ohm transmission lines

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

CD54/74AC04, CD54/74AC05 CD54/74ACT04, CD54/74ACT05

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A :	-55	+125	°C
Input Rise and Fall Slew Rate, dV/dt :			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V_{IL}		1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage (04)	V_{OH}	V_{IH}	-0.05	1.5	1.4	—	1.4	—	1.4	V
			-0.05	3	2.9	—	2.9	—	2.9	
			-0.05	4.5	4.4	—	4.4	—	4.4	
		V_{IL}	-4	3	2.58	—	2.48	—	2.4	
			-24	4.5	3.94	—	3.8	—	3.7	
			-75	5.5	—	—	3.85	—	—	
			-50	5.5	—	—	—	—	3.85	
Low-Level Output Voltage	V_{OL}	V_{IH}	0.05	1.5	—	0.1	—	0.1	—	V
			0.05	3	—	0.1	—	0.1	—	
			0.05	4.5	—	0.1	—	0.1	—	
		V_{IL}	12	3	—	0.36	—	0.44	—	
			24	4.5	—	0.36	—	0.44	—	
			75	5.5	—	—	—	1.65	—	
			50	5.5	—	—	—	—	1.65	
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1 μ A
Quiescent Supply Current, SSI	I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80 μ A

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC04, CD54/74AC05

CD54/74ACT04, CD54/74ACT05

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V _{IH} (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (04)	V _{OH}	V _{IH} or V _{IL} #, *	-0.05 -24 -75 -50	4.5 4.5 5.5 5.5	4.4 3.94 — —	— 3.8 3.85 —	4.4 3.7 — 3.85	— — — —	— — — —	V
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05 24 75 50	4.5 4.5 5.5 5.5	— — — —	0.1 0.36 — —	0.1 0.44 1.65 —	— — — —	0.1 0.5 — 1.65	V
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1 μA
Quiescent Supply Current, SSI	I _{CC}	V _{CC} or GND	0	5.5	—	4	—	40	—	80 μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3 mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
nA	0.18

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

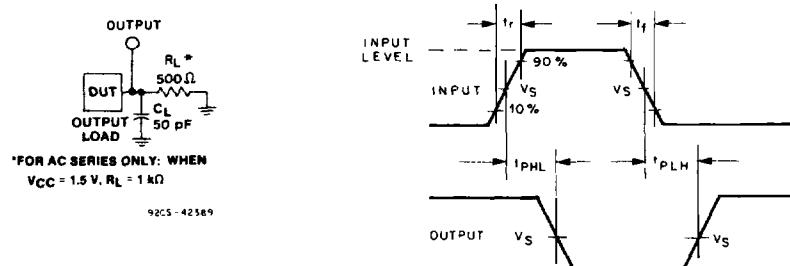


Fig. 1 - Propagation delay times and test circuit - AC/ACT04.

	CD54/74AC	CD54/74ACT
Input Level	V _{CC}	3 V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5 V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}

CD54/74AC04, CD54/74AC05 CD54/74ACT04, CD54/74ACT05

SWITCHING CHARACTERISTICS: AC Series; $t_i, t_r = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: Input to Output (04)	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 2.3 1.7	74 10.4 5.9	— 2.3 1.6	81 9.1 6.5	ns	
High Z to Output Low (05)	t_{PZL}	1.5 3.3 5	— 2.3 1.7	74 10.4 5.9	— 2.3 1.6	81 9.1 6.5	ns	
Output Low to High Z (05)	t_{PLZ}	1.5 3.3 5	— 3 2.2	94 10.4 7.5	— 2.9 2.1	103 11.5 8.2	ns	
Power Dissipation Capacitance	$C_{PD\$}$	—	105 Typ.		105 Typ.		pF	
Input Capacitance	C_I	—	—	10	—	10	pF	

SWITCHING CHARACTERISTICS: ACT Series; $t_i, t_r = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: Input to Output (04)	t_{PLH} t_{PHL}	5†	2.4	8.5	2.3	9.3	ns	
Output Low to High Z	t_{PLZ}	5	2.8	9.8	2.7	10.8	ns	
High Z to Output Low (05)	t_{PZL}	5	2.4	8.5	2.3	9.3	ns	
Power Dissipation Capacitance	$C_{PD\$}$	—	105 Typ.		105 Typ.		pF	
Input Capacitance	C_I	—	—	10	—	10	pF	

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

$\$C_{PD}$ is used to determine the dynamic power consumption, per inverter.

For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_I)$

For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$, where f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage.

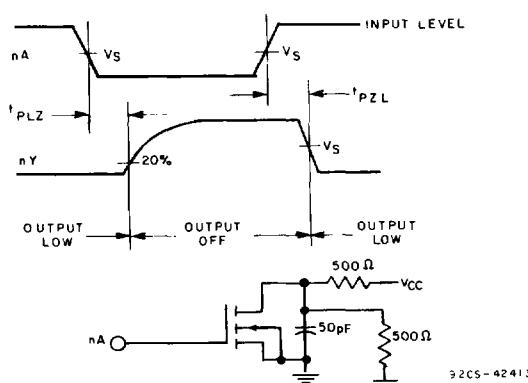


Fig. 2 - Propagation delay times and test circuit - AC/ACT05

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}