

54ACT823 9-Bit D Flip-Flop

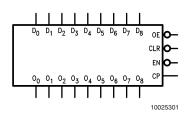
General Description

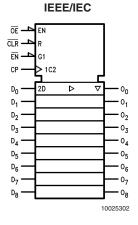
The ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

Features

- Outputs source/sink 24 mA
- TRI-STATE outputs for bus interfacing
- Inputs and outputs are on opposite sides
- ACT823 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-9161001

Logic Symbols

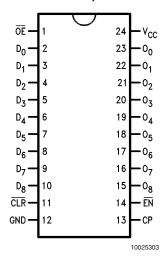




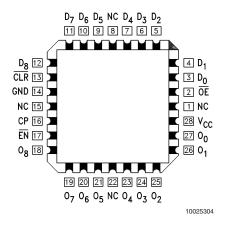
Pin Names	Description
D_0 - D_8	Data Inputs
$D_0 - D_8$ $D_0 - O_8$	Data Outputs
ŌĒ	Output Enable
CLR	Clear
CP	Clock Input
EN	Clock Enable

Connection Diagrams

Pin Assignment for DIP and Cerpack



Pin Assignment for LCC



Functional Description

The ACT823 consists of nine D-type edge-triggered flipflops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the

state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{\text{CLR}}$ is LOW and $\overline{\text{OE}}$ is LOW, the outputs are LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the flip-flops. When $\overline{\text{EN}}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{\text{EN}}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

		Inputs			Internal	Output	Function
ŌĒ	CLR	EN	CP	D	Q	0	
Н	Х	L	N	L	L	Z	High Z
Н	Χ	L	Ν	Н	Н	Z	High Z
Н	L	Χ	Χ	Χ	L	Z	Clear
L	L	Χ	Χ	Χ	L	L	Clear
Н	Н	Н	Χ	Χ	NC	Z	Hold
L	Н	Н	Χ	Χ	NC	NC	Hold
Н	Н	L	N	L	L	Z	Load
Н	Н	L	Ν	Н	Н	Z	Load
L	Н	L	Ν	L	L	L	Load
L	Н	L	N	Н	Н	Н	Load

H = HIGH Voltage Level

L = LOW Voltage Level

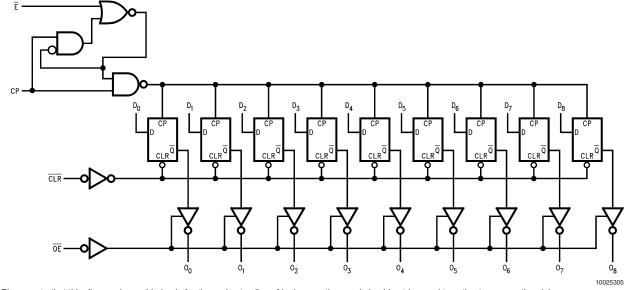
X = Immaterial

Z = High Impedance

N = LOW-to-HIGH Transition

NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) -0.5V to 7.0V

DC Input Diode Current (IIK)

DC Output Diode Current (IOK)

 $V_{O} = -0.5V$ -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) -0.5V to V_{CC} + 0.5V

DC Output Source or Sink

Current

 (I_{O}) ±50 mA

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ± 50 mA Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C

Junction Temperature (T_J)

CDIP 175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

 $\begin{array}{lll} \text{ACT} & \text{4.5V to 5.5V} \\ \text{Input Voltage (V_I)} & \text{0V to V}_{\text{CC}} \\ \text{Output Voltage (V}_{\text{O}}) & \text{0V to V}_{\text{CC}} \\ \end{array}$

Operating Temperature (T_A)

54ACT -55°C to +125°C

Minimum Input Edge Rate $(\Delta V/\Delta t)$

ACT Devices

 V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V _{cc}	T _A =	Units	Conditions
		(V)	-55°C to +125°C		
V _{IH}	Minimum High Level	4.5	2.0	V	V _{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V _{CC} -0.1V
V _{IL}	Maximum Low Level	4.5	0.8	V	V _{OUT} = 0.1V
	Input Voltage	4.5	0.8		or V _{CC} -0.1V
V _{OH}	Minimum High Level	4.5	3.7	V	$I_{OH} = -24 \text{ mA}$
	Output Voltage			V	
V_{OL}	Maximum Low Level	4.5	0.5	V	I _{OL} = 24 mA
	Output Voltage			· ·	
I _{IN}	Maximum Input Leakage	5.5	±1.0	μA	$V_{I} = V_{CC}$, GND
	Current	5.5	±1.0	μA	VI = VCC, GIVE
l _{oz}	Maximum TRI-STATE	5.5	±10.0	μΑ	$V_I = V_{IL}, V_{IH}$
	Current				$V_O = V_{CC}$, GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} -2.1V$
I _{OLD}	(Note 3) Minimum	5.5	50	mA	V _{OLD} = 1.65V Max
	Dynamic Output	5.5	-50	mA	V _{OHD} = 3.85V Min
I _{OHD}	Current	5.5	-50	IIIA	v _{OHD} = 3.63 v iviii1
I _{CC}	Maximum Quiescent	5.5	160	μA	$V_{IN} = V_{CC}$
	Supply Current				or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 4)	$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $C_L = 50 \text{ pF}$		Units	Fig. No.
			Min	Max		
f _{max}	Maximum Clock Frequency	5.0	95		MHz	

AC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V) (Note 4)	$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $C_L = 50 \text{ pF}$		Units	Fig. No.
			Min	Max		
t _{PLH}	Propagation Delay	5.0	1.0	12.0	ns	
	CP to O _n					
t _{PHL}	Propagation Delay	5.0	1.0	12.0	ns	
	CP to O _n					
t _{PHL}	Propagation Delay	5.0	1.0	18.0	ns	
	CLR to O _n					
t _{PZH}	Output Enable Time	5.0	1.0	11.5	ns	
	OE to O _n					
t _{PZL}	Output Enable Time	5.0	1.0	12.0	ns	
	OE to O _n					
t _{PHZ}	Output Disable Time	5.0	1.0	13.5	ns	
	ŌĒ to O _n					
t _{PLZ}	Output Disable Time	5.0	1.0	12.0	ns	
	ŌĒ to O _n					

Note 4: Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	V _{cc} (V)	$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$	Units	Fig.
		(Note 5)	$C_L = 50 pF$		
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW	5.0	4.0	ns	
	D to CP				
t _h	Hold Time, HIGH or LOW	5.0	3.0	ns	
	D _n to CP				
t _s	Setup Time, HIGH or LOW	5.0	4.0	ns	
	EN to CP				
t _h	Hold Time, HIGH or LOW	5.0	3.0	ns	
	EN to CP				
t _w	CP Pulse Width	5.0	6.0	ns	
	HIGH or LOW				
t _w	CLR Pulse Width, LOW	5.0	7.5	ns	
t _{rec}	CLR to CP	5.0	4.5	ns	
	Recovery Time				

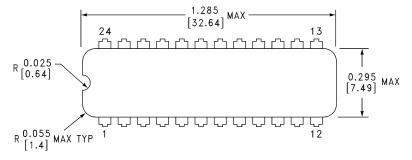
Note 5: Voltage Range 5.0 is 5.0V ± 0.5 V

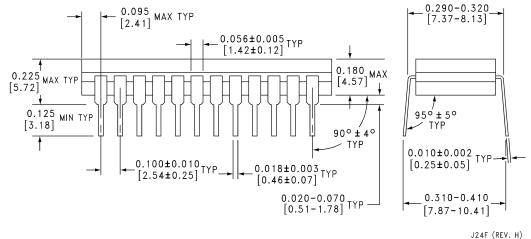
Capacitance

Symbol	Parameter	Max	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	4.4	pF	V _{CC} = 5.0V

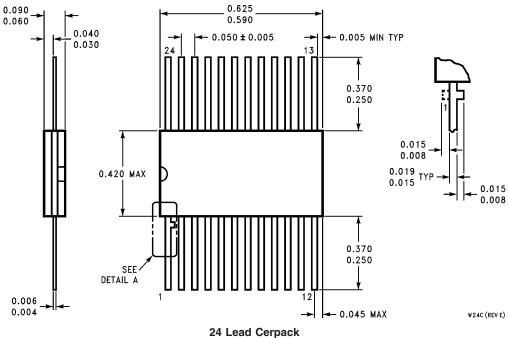
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Physical Dimensions inches (millimeters) unless otherwise noted





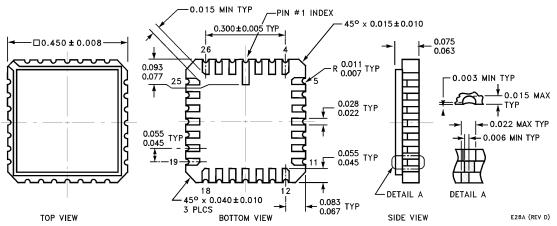
24 Lead Ceramic Dual-in-line Package Number J24F



24 Lead Cerpack
Package Number W24C

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28 Lead Ceramic Leadless Chip Carrier Package Number E28A

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