Signetics

54F38
Buffer

Quad Two-Input NAND Buffer (Open Collector)

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUTS
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F38/BCA
Ceramic Flat Pack	54F38/BDA
Ceramic LLCC	54F38/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Outputs	OC*/80	OC*/48mA

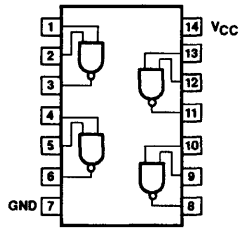
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.
*OC = Open Collector

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

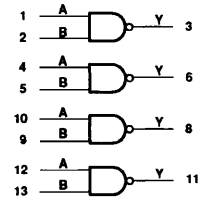
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	128	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_{OH} = Max				250	µA
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 48mA			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at others maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			5	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.6	-1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		4	7	mA
		I_{CCL}		$V_I \geq 4.0V$		22	30	mA

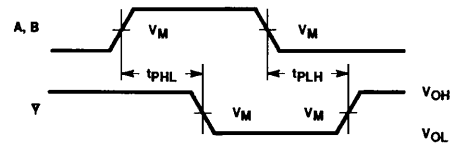
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	7.5	10	12.5	7.0	14.5	ns
t_{PHL}	A, B to $\overline{Y}$		1.5	3.0	5.0	1.0	6.0	ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When using open collector parts, the value of the pull-up resistor greatly affects the value of the TPLH. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the TPLH up to 50% with only a slight increase in the TPHL. However, if the value of the pull-up resistor is changed, the user must make certain that the total IOL current through the resistor, plus the total IIL's of the receivers does not exceed the IOL maximum specification.

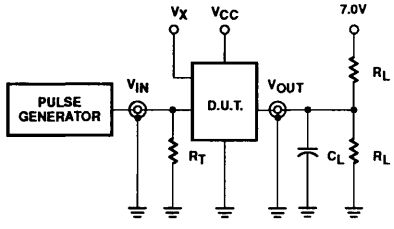
AC WAVEFORM



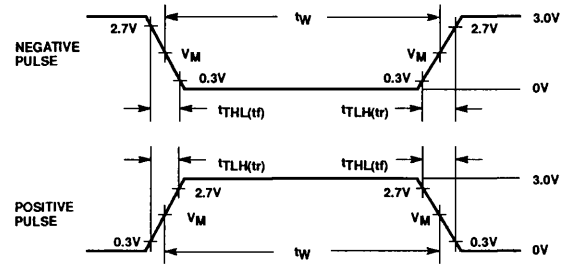
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collecor Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns