

TC74LCX245F/FW/FS

Low Voltage Octal Bus Transceiver with 5V Tolerant Inputs and Outputs

The TC74LCX245 is a high performance CMOS OCTAL BUS TRANSCIEVER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

The direction of data transmission is determined by the level of the DIR input. The enable input (\overline{OE}) can be used to disable the device so that the busses are effectively isolated.

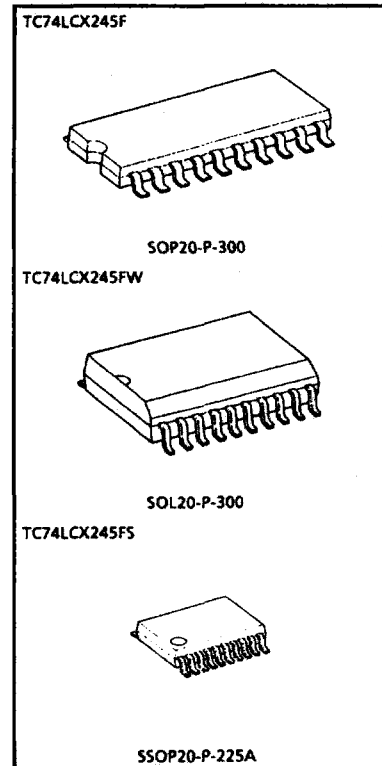
All inputs are equipped with protection circuits against static discharge.

Features

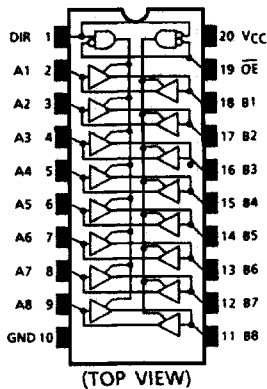
- Low Voltage Operation: $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation: $t_{pd} = 7.0ns$ (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output Current: $I_{OH}/I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)
- Latch-up Performance: $\pm 500mA$
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Bidirectional interface between 5V and 3.3V signals.
- Power down protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series
- (74AC/VHC/HC/F/ALS/LS etc.) 245 type.

(Note) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

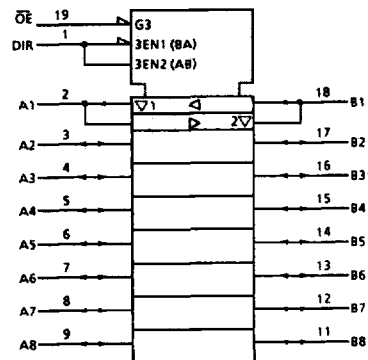
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.



Weight SOP20-P-300 : 0.22g (Typ.)
SOL20-P-300 : 0.46g (Typ.)
SSOP20-P-225A : 0.09g (Typ.)



Pin Assignment



IEC Logic Symbol

Truth Table

Inputs		Output	Function	
\overline{OE}	DIR		A Bus	B Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High Impedance	

X: Don't Care

Z: High Impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage (DIR, \overline{G})	V_{IN}	-0.5 ~ 7.0	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5 ~ 7.0 (Note 1) -0.5 ~ $V_{CC} + 0.5$ (Note 2)	V
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC} /Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	-65 ~ 150	°C

(Note 1) $V_{CC} = 0V$ (Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 ~ 3.6 1.5 ~ 3.6 (Note 4)	V
Input Voltage (DIR, \overline{OE})	V_{IN}	0 ~ 5.5	V
Bus I/O Voltage	$V_{I/O}$	0 ~ 5.5 (Note 5) 0 ~ V_{CC} (Note 6)	V
Output Current	I_{OH}/I_{OL}	±24 (Note 7) ±12 (Note 8)	mA
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 10 (Note 9)	ns/V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6V$ (Note 8) $V_{CC} = 2.7 \sim 3.0V$ (Note 9) $V_{IN} = 0.8 \sim 2.0V$, $V_{CC} = 3.0V$

Electrical Characteristics

DC Characteristics (Ta = -40 ~ 85°C)

Parameter	Symbol	Test Condition		V _{CC} (V)	Min.	Max.	Unit	
Input Voltage	"H" level	V _{IH}		2.7 - 3.6	2.0	-	V	
	"L" level	V _{IL}		2.7 - 3.6	-	0.8	V	
Output Voltage	"H" level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100µA	2.7 - 3.6	V _{CC} - 0.2	-	V
				I _{OH} = -12mA	2.7	2.2	-	
				I _{OH} = -18mA	3.0	2.4	-	
				I _{OH} = -24mA	3.0	2.2	-	
"L" level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100µA	2.7 - 3.6	-	0.2	V	
			I _{OL} = 12mA	2.7	-	0.4		
			I _{OL} = 16mA	3.0	-	0.4		
			I _{OL} = 24mA	3.0	-	0.55		
Input Leakage Current	I _{IN}		V _{IN} = 0 - 5.5V	2.7 - 3.6	-	±5.0	µA	
3-State Output Off-State Current	I _{OZ}		V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 - 5.5V	2.7 - 3.6	-	±5.0	µA	
Power Off Leakage Current	I _{OFF}		V _{IN} /V _{OUT} = 5.5V	0	-	10.0	µA	
Quiescent Supply Current	I _{CC}		V _{IN} = V _{CC} or GND	2.7 - 3.6	-	10.0	µA	
			V _{IN} /V _{OUT} = 3.6-5.5V	2.7 - 3.6	-	±10.0		
Increase in I _{CC} per Input	ΔI _{CC}		V _{IH} = V _{CC} - 0.6V	2.7 - 3.6	-	500	µA	

AC Characteristics (Ta = -40 ~ 85°C)

Parameter	Symbol	Test Condition	V _{CC} (V)	Min.	Max.	Unit
Propagation Delay Time	t _{pLH} t _{pHL}	(Fig. 1, 2)	2.7	–	8.0	ns
			3.3±0.3	1.5	7.0	
Output Enable Time	tpZL tpZH	(Fig. 1, 3)	2.7	–	9.5	ns
			3.3±0.3	1.5	8.5	
Output Disable Time	tpLZ tpHZ	(Fig. 1, 3)	2.7	–	8.5	ns
			3.3±0.3	1.5	7.5	
Output to Output Skew	tosLH tosHL	(Note 10)	2.7	–	1.0	ns
			3.3±0.3	–	1.0	

(Note 10) Parameter guaranteed by design. (t_{osLH} = t_{pLHm} - t_{pLHn}, t_{osHL} = t_{pHLm} - t_{pHLn})

Dynamic Switching Characteristics (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

Parameter	Symbol	Test Condition	V _{CC} (V)	Typical	Unit
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

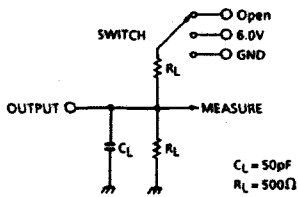
Capacitive Characteristics (Ta = 25°C)

Parameter	Symbol	Test Condition	V _{CC} (V)	Typical	Unit
Input Capacitance	C _{IN}	DIR, OE	3.3	7	pF
Bus Input Capacitance	C _{ID}	An, Bn	3.3	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation: I_{CC(opr.)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/8 (per bit)

TEST CIRCUIT

Fig.1



Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND

AC WAVEFORM

Fig.2 tpLH, tpHL

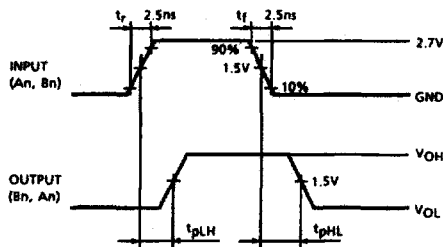
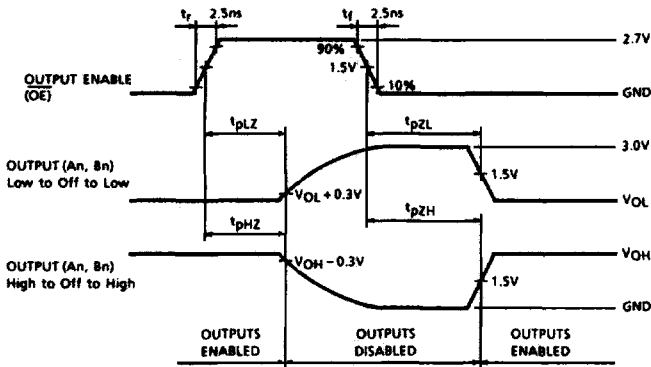


Fig.3 tpLZ, tpHZ, tpZL, tpZH



Notes

1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Department of Commerce prior to export. Any export or re-export, directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.

2. **LIFE SUPPORT POLICY**

Toshiba products described in this document are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

A critical component in any component of a life support system whose failure to perform may cause a malfunction of the life support system, or may affect its safety or effectiveness.

3. The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this data book is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.