To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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RENESAS

R8A66165SP / R8A66166SP / R8A66167SP / R8A66168SP
n-BIT HIGH VOLTAGE OUTPUT LED DRIVER WITH SHIFT REGISTER AND LATCH

REJ03F0281-0101
Rev. 1.01
Dec. 15. 2008

DESCRIPTION

R8A66165～R8A66168 are high voltage LED array driver having n-bit serial input and parallel output shift register function with direct coupled reset input and output latch function.

These products guarantees the output current of 24mA which is sufficient for anode common LED drive, capable of following n-bits continuously at the same time. Parallel output is 24V high voltage open drain output.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

The product part number and the parallel data outputs number are shown in the following table.

| Part number	Parallel data outputs number n	$\overline{Q1}$～$\overline{Qn}$	SQn
R8A66165SP	8-Bit	$\overline{Q1}$～$\overline{Q8}$	SQ8
R8A66166SP	16-Bit	$\overline{Q1}$～$\overline{Q16}$	SQ16
R8A66167SP	24-Bit	$\overline{Q1}$～$\overline{Q24}$	SQ24
R8A66168SP	32-Bit	$\overline{Q1}$～$\overline{Q32}$	SQ32

FEATURES

- Anode common LED drive
- V_{CC} 5V or 3.3V single power supply
- High voltage, High output current: all parallel outputs $\overline{Q1}$～$\overline{Qn}$ V_O =24V high voltage, I_{OL} =24mA simultaneous lighting available
- Low power dissipation: 100uW/package (max) (V_{CC} =5.0V, Ta =25℃, quiescent state)
- High noise margin: Schmitt input circuit provides responsiveness to a long line length
- Equipped with direct-coupled reset
- Open drain output: (except serial data output SQn)
- Wide operating temperature range: Ta = -40℃~+85℃

APPLICATION

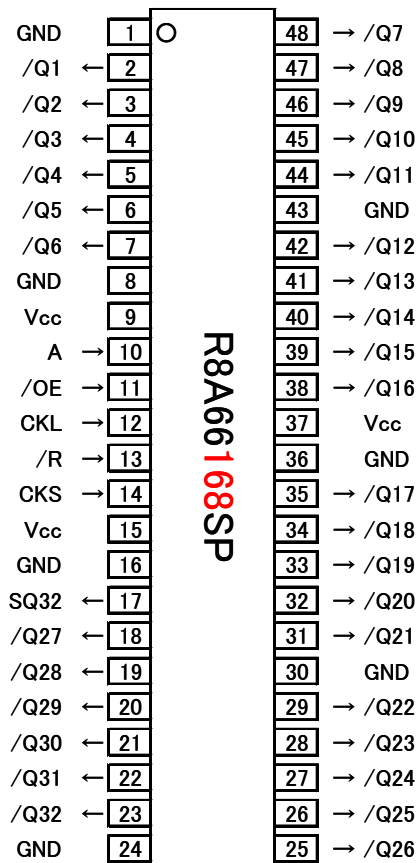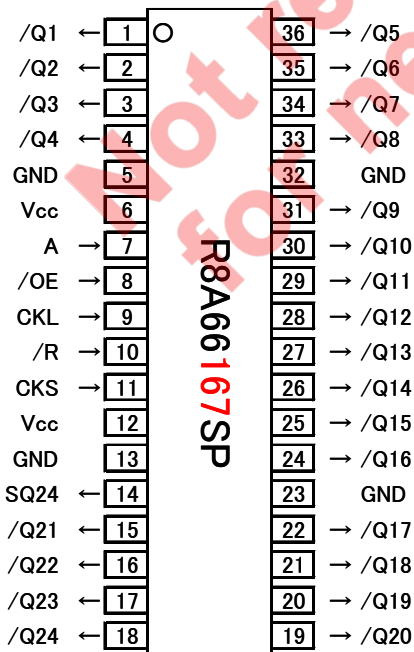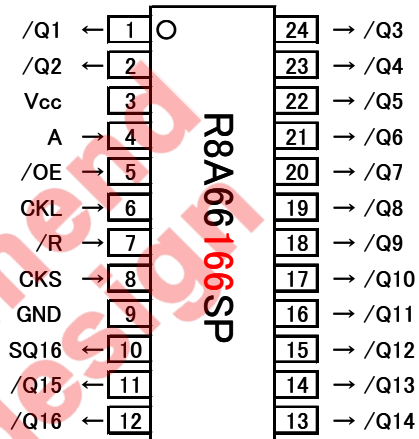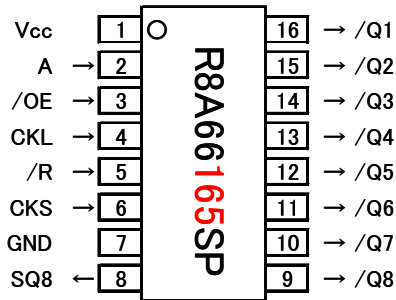- LED array drive, The various high voltage LED display modules

BLOCK DIAGRAM
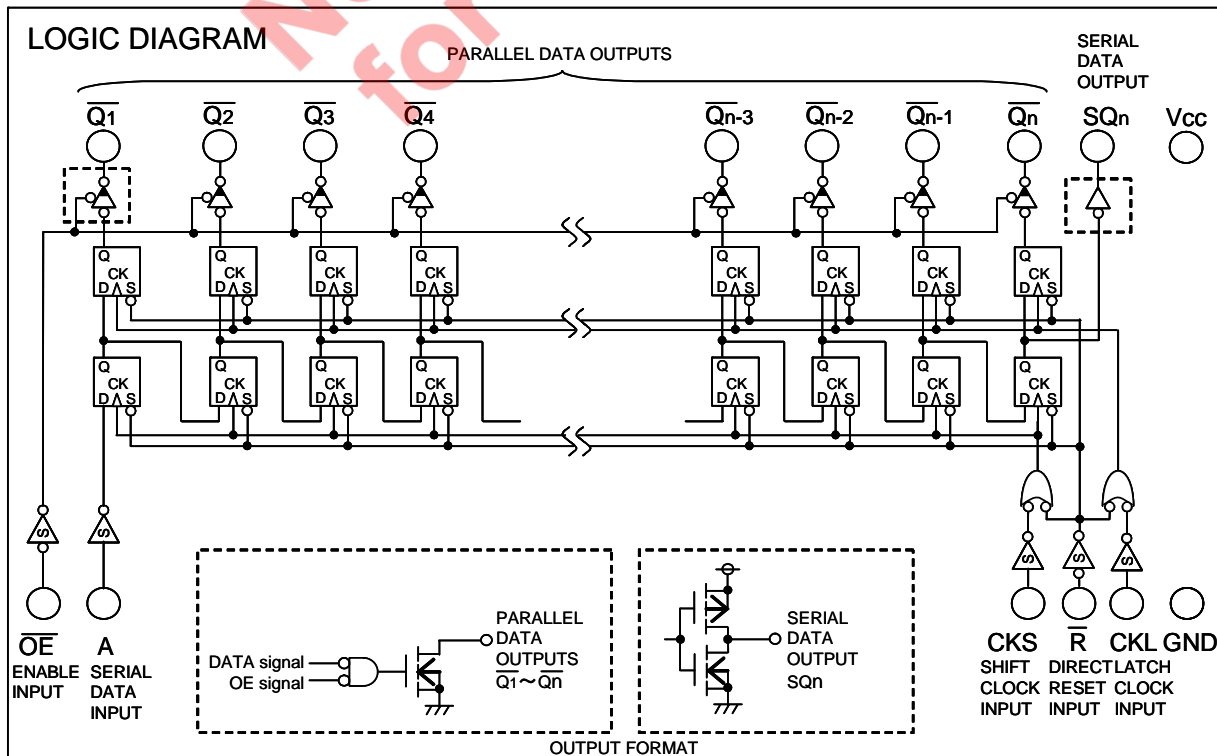
PIN SPECIFICATION

Pin Name	Symbol	In/Out	R8A66165SP 8-BIT	R8A66166SP 16-BIT	R8A66167SP 24-BIT	R8A66168SP 32-BIT
DIRECT RESET INPUT	/R	Input	1	1	1	1
SERIAL DATA INPUT	A	Input	1	1	1	1
SHIFT CLOCK INPUT	CKS	Input	1	1	1	1
LATCH CLOCK INPUT	CKL	Input	1	1	1	1
ENABLE INPUT	/OE	Input	1	1	1	1
PARALLEL DATA OUTPUTS	/Q1∼/Qn	Output	8	16	24	32
SERIAL DATA OUTPUT	SQn	Output	1	1	1	1
Vcc	Vcc	-	1	1	2	3
GND	GND	-	1	1	4	7
Total pin count			16	24	36	48

PIN CONFIGURATION (TOP VIEW)

R8A66165SP

Left	Pin		Pin	Right
Vcc	1		16	→ /Q1
A →	2		15	→ /Q2
/OE →	3		14	→ /Q3
CKL →	4		13	→ /Q4
/R →	5		12	→ /Q5
CKS →	6		11	→ /Q6
GND	7		10	→ /Q7
SQ8 ←	8		9	→ /Q8

R8A66166SP

Left	Pin		Pin	Right
/Q1 ←	1		24	→ /Q3
/Q2 ←	2		23	→ /Q4
Vcc	3		22	→ /Q5
A →	4		21	→ /Q6
/OE →	5		20	→ /Q7
CKL →	6		19	→ /Q8
/R →	7		18	→ /Q9
CKS →	8		17	→ /Q10
GND	9		16	→ /Q11
SQ16 ←	10		15	→ /Q12
/Q15 ←	11		14	→ /Q13
/Q16 ←	12		13	→ /Q14

R8A66167SP

Left	Pin		Pin	Right
/Q1 ←	1		36	→ /Q5
/Q2 ←	2		35	→ /Q6
/Q3 ←	3		34	→ /Q7
/Q4 ←	4		33	→ /Q8
GND	5		32	GND
Vcc	6		31	→ /Q9
A →	7		30	→ /Q10
/OE →	8		29	→ /Q11
CKL →	9		28	→ /Q12
/R →	10		27	→ /Q13
CKS →	11		26	→ /Q14
Vcc	12		25	→ /Q15
GND	13		24	→ /Q16
SQ24 ←	14		23	GND
/Q21 ←	15		22	→ /Q17
/Q22 ←	16		21	→ /Q18
/Q23 ←	17		20	→ /Q19
/Q24 ←	18		19	→ /Q20

R8A66168SP

Left	Pin		Pin	Right
GND	1		48	→ /Q7
/Q1 ←	2		47	→ /Q8
/Q2 ←	3		46	→ /Q9
/Q3 ←	4		45	→ /Q10
/Q4 ←	5		44	→ /Q11
/Q5 ←	6		43	GND
/Q6 ←	7		42	→ /Q12
GND	8		41	→ /Q13
Vcc	9		40	→ /Q14
A →	10		39	→ /Q15
/OE →	11		38	→ /Q16
CKL →	12		37	Vcc
/R →	13		36	GND
CKS →	14		35	→ /Q17
Vcc	15		34	→ /Q18
GND	16		33	→ /Q19
SQ32 ←	17		32	→ /Q20
/Q27 ←	18		31	→ /Q21
/Q28 ←	19		30	GND
/Q29 ←	20		29	→ /Q22
/Q30 ←	21		28	→ /Q23
/Q31 ←	22		27	→ /Q24
/Q32 ←	23		26	→ /Q25
GND	24		25	→ /Q26

RENESAS

FUNCTIONAL DESCRIPTION

As R8A66165~R8A66168 uses silicon gate CMOS process. It realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shift register consists of two flip-flop having independent clocks for shifting and latching.

As for clock input, shift clock input CKS and latch clock input CKL are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shift register and the signal of A shifts shifting registers one by one when a pulse is impressed to CKS. When A is "H", the signal of "L" shifts.

When the pulse is impressed to CKL, the contents of the shifting register at that time are stored in a latching register, and they appear in the parallel data outputs from $\overline{Q1} \sim \overline{Qn}$.

Outputs $\overline{Q1} \sim \overline{Qn}$ are 24V high voltage open drain outputs.

To extend the number of bits, use the serial data output SQn which shows the output of the shifting register of the last n bit.

When reset input $\overline{R}$ is changed to "L", $\overline{Q1} \sim \overline{Qn}$ and SQn are reset. In this case, shifting and latching register are set.

If "H" is impressed to output enable input $\overline{OE}$, $\overline{Q1} \sim \overline{Qn}$ reaches the high impedance state, but SQn does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

FUNCTION TABLE (Note 1)

Operation mode		Input					Parallel data output									Serial data output SQn	Remarks
		$\overline{R}$	CKS	CKL	A	$\overline{OE}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	------	$\overline{Qn-3}$	$\overline{Qn-2}$	$\overline{Qn-1}$	$\overline{Qn}$		
Reset		L	X	X	X	X	Z	Z	Z	Z	------	Z	Z	Z	Z	L	—
Shift Latch operation	Shift t_1	H	↑	X	H	L	$\overline{Q1}^0$	$\overline{Q2}^0$	$\overline{Q3}^0$	$\overline{Q4}^0$	------	$\overline{Qn-3}^0$	$\overline{Qn-2}^0$	$\overline{Qn-1}^0$	$\overline{Qn}^0$	q_{n-1}^0	Output Lighting "H"
	Latch t_2	H	X	↑	X	L	L	q_1^0	q_2^0	q_3^0	------	q_{n-4}^0	q_{n-3}^0	q_{n-2}^0	q_{n-1}^0	q_{n-1}^0	
	Shift t_1	H	↑	X	L	L	$\overline{Q1}^0$	$\overline{Q2}^0$	$\overline{Q3}^0$	$\overline{Q4}^0$	------	$\overline{Qn-3}^0$	$\overline{Qn-2}^0$	$\overline{Qn-1}^0$	$\overline{Qn}^0$	q_{n-1}^0	Output Lights-out "L"
	Latch t_2	H	X	↑	X	L	Z	q_1^0	q_2^0	q_3^0	------	q_{n-4}^0	q_{n-3}^0	q_{n-2}^0	q_{n-1}^0	q_{n-1}^0	
Output disable		X	X	X	X	H	Z	Z	Z	Z	------	Z	Z	Z	Z	q_n	—

Note1: ↑ : Change from low-level to high-level
$\overline{Q}^0$: Output state $\overline{Q}$ before CKL changed
X : Irrelevant
q^0 : Contents of shift register before CKS changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (Ta=-40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
VCC	Supply voltage			−0.5～＋7.0	V
VI	Input voltage			−0.5～VCC+0.5	V
VO	Output voltage	$\overline{Q1}$～$\overline{Qn}$		−0.5～＋27	V
		SQn		−0.5～VCC+0.5	V
IO	Output current per	$\overline{Q1}$～$\overline{Qn}$		50	mA
	Output pin	SQn		±25	
ICC	Supply / GND current	R8A66165SP	VCC、GND	−20、+220	mA
		R8A66166SP		−20、+410	
		R8A66167SP		−20、+600	
		R8A66168SP		−20、+790	
Pd	Power dissipation	R8A66165SP		500	mW
		R8A66166SP		500	
		R8A66167SP		650	
		R8A66168SP		650	
Tstg	Storage temperature range			−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Supply voltage	5.0V support	4.5	5.0	5.5	V
		3.3V support	3.0	3.3	3.6	V
VI	Input voltage		0		VCC	V
VO	Output voltage	SQn	0		VCC	V
		$\overline{Q1}$～$\overline{Qn}$ IOZH≦10uA	0		24	V
Topr	Operating temperature range		−40		85	℃

ELECTRICAL CHARACTERISTICS (Ta=-40~+85℃,VCC=3.0~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
VT+	Positive-going threshold voltage	VO=0.1V, VCC-0.1V		0.48xVCC		0.70xVCC	V
VT−	Negative-going threshold voltage	VO=0.1V, VCC-0.1V		0.20xVCC		0.46xVCC	V
VOL	Low-level output voltage $\overline{Q1}$～$\overline{Qn}$	VI=VT+,VT-	IOL=24mA (Note 3)			0.55	V
VOH	High-level output voltage SQn	VI=VT+,VT-	IOH=-4mA	VCC-0.40			V
VOL	Low-level output voltage SQn	VI=VT+,VT-	IOL=4mA			0.40	V
IIH	High-level input current	VI=VCC				5	uA
IIL	Low-level input current	VI=GND				-5	uA
IOZ	Off-state output leak current $\overline{Q1}$～$\overline{Qn}$	VI=VT+,VT-	VO=0~24V			±10	uA
ICC	Quiescent supply current	VI=VCC,GND				1	mA

Note2 : ELECTRICAL CHARACTERISTICS (except ICC) above is the specification per a pin.

Note3 : Each pin of $\overline{Q1}$～$\overline{Qn}$ guarantees IOL=24mA.
   Simultaneous lighting of all n-bits is available both for dynamic and static lighting.

SWITCHING CHARACTERISTICS (Ta=-40~+85℃,Vcc=5.0V or 3.3V)

Symbol	Parameter		Test conditions	5.0V specification			3.3V specification			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
fmax	Maximum clock frequency					4			3.3	MHz
tPLH	Output "L-H" and "H-L"	CKS-SQn				125			150	ns
tPHL	propagation time					125			150	ns
tPHL	Output "H-L" propagation time	$\overline{R}$-SQn	C$_L$=50pF			125			150	ns
tPLZ	Output "L-Z" propagation time	$\overline{R}$-$\overline{Q1}$~$\overline{Qn}$ (turned off)	R$_L$=1KΩ			200			220	ns
tPZL	Output "Z-L" propagation time	CKL-$\overline{Q1}$~$\overline{Qn}$ (turned on)	(Note 4)			125			150	ns
tPLZ	Output "L-Z" propagation time	CKL-$\overline{Q1}$~$\overline{Qn}$ (turned off)				200			220	ns
tPZL	Output "Z-L" propagation time	$\overline{OE}$-$\overline{Q1}$~$\overline{Qn}$ (turned on)				125			150	ns
tPLZ	Output "L-Z" propagation time	$\overline{OE}$-$\overline{Q1}$~$\overline{Qn}$ (turned off)				200			220	ns
Cl	Input capacitance					10			10	pF

TIMING REQUIREMENTS (Ta=-40~+85℃,Vcc=5.0V or 3.3V)

Symbol	Parameter	Test conditions	5.0V specification			3.3V specification			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
tw	CKS,CKL,$\overline{R}$ pulse width		125			150			ns
tsu	A setup time with respect to CKS		125			150			ns
tsu	CKS setup time with respect to CKL	(Note 4)	125			150			ns
th	A hold time with respect to CKS		15			20			ns
trec	$\overline{R}$ recovery time with respect to CKS, CKL		70			80			ns

Note 4 : Test Circuit
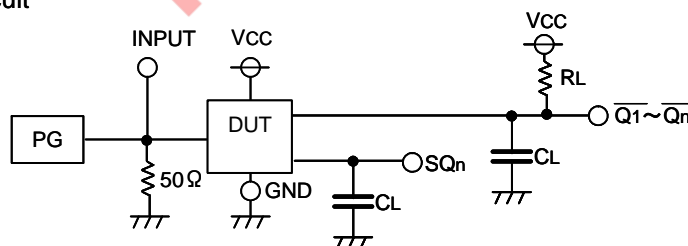
(1) The pulse generator (PG) has the following characteristics (10%~90%). :tr = 6ns, tf = 6ns.
(2) The capacitance C$_L$ includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM
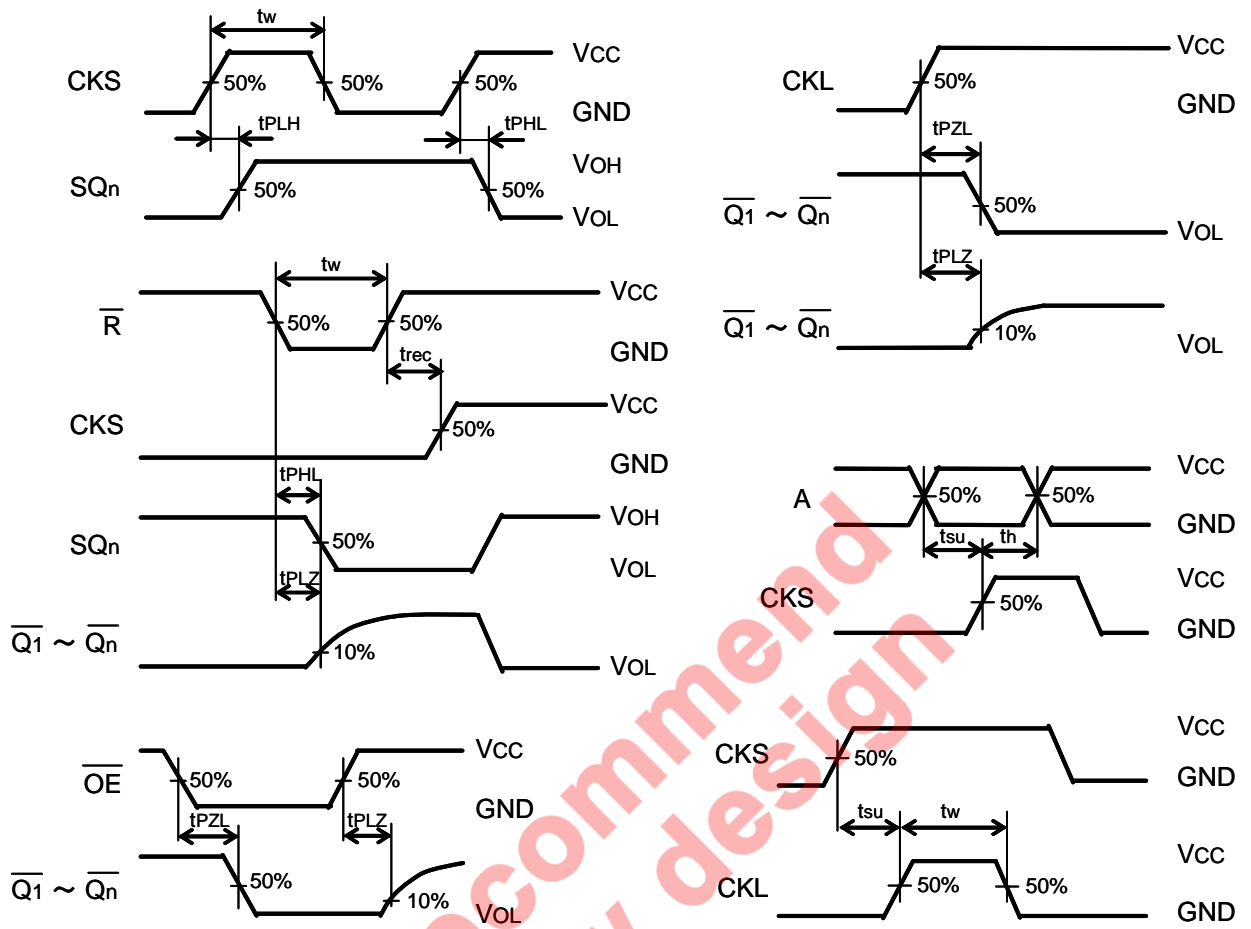
PACKAGE OUTLINE

Product part number	Package	RENESAS Code	Previous Code
R8A66165SP	16pin SOP	PRSP0016DJ-A	16P2X-E
R8A66166SP	24pin SOP	PRSP0024DF-A	24P2X-B
R8A66167SP	36pin SSOP	PRSP0036GC-A	36P2X-B
R8A66168SP	48pin SSOP	PRSP0048ZB-A	48P2X-A

R8A66165SP

PRSP0016DJ-A

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.55
D	9.80	9.90	10.00
E	3.80	3.90	4.00
HE	5.80	6.00	6.20
b	0.33	—	0.51
c	0.19	—	0.25
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
θ	0°	—	8°
ZD	—	0.505	—
Lp	0.40	—	—
L1	—	1.05	—

Index mark

Detail F
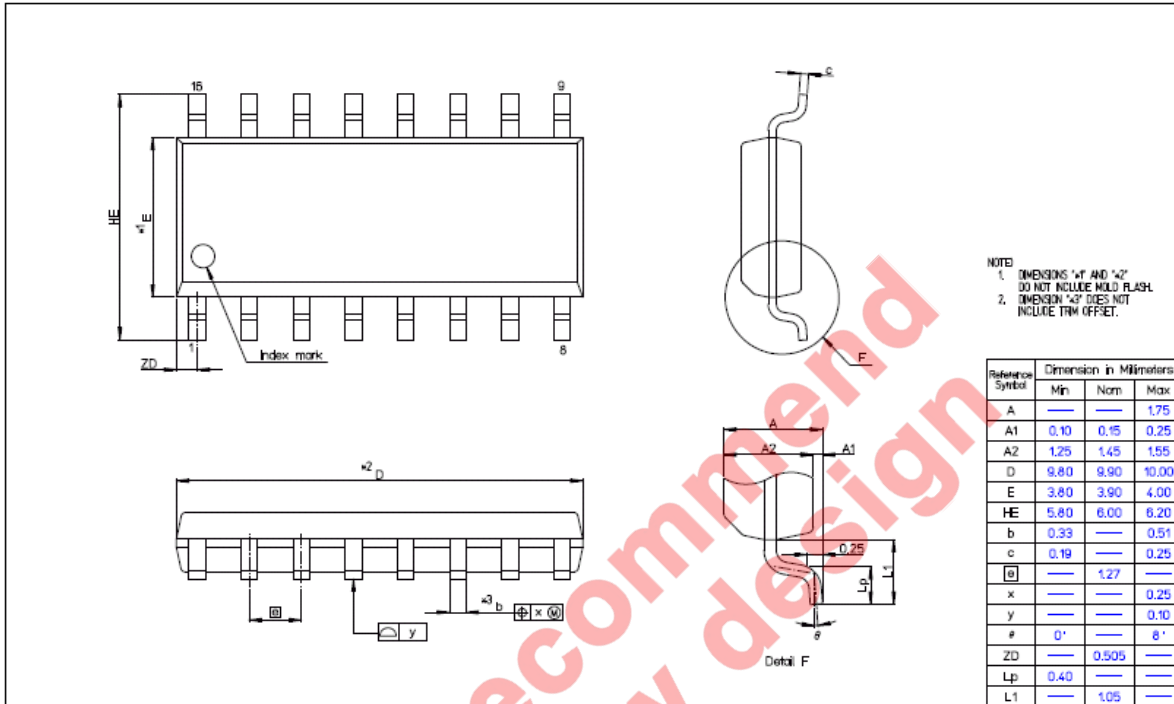
R8A66166SP

PRSP0024DF-A

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.19	15.39	15.49
E	7.39	7.49	7.59
A2	—	2.34	—
A1	0.10	0.20	0.30
A	—	—	2.65
bp	0.31	0.41	0.51
c	0.20	0.25	0.33
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.71	—
Lp	0.38	—	—
L1	—	1.41	—

Index mark

Detail F
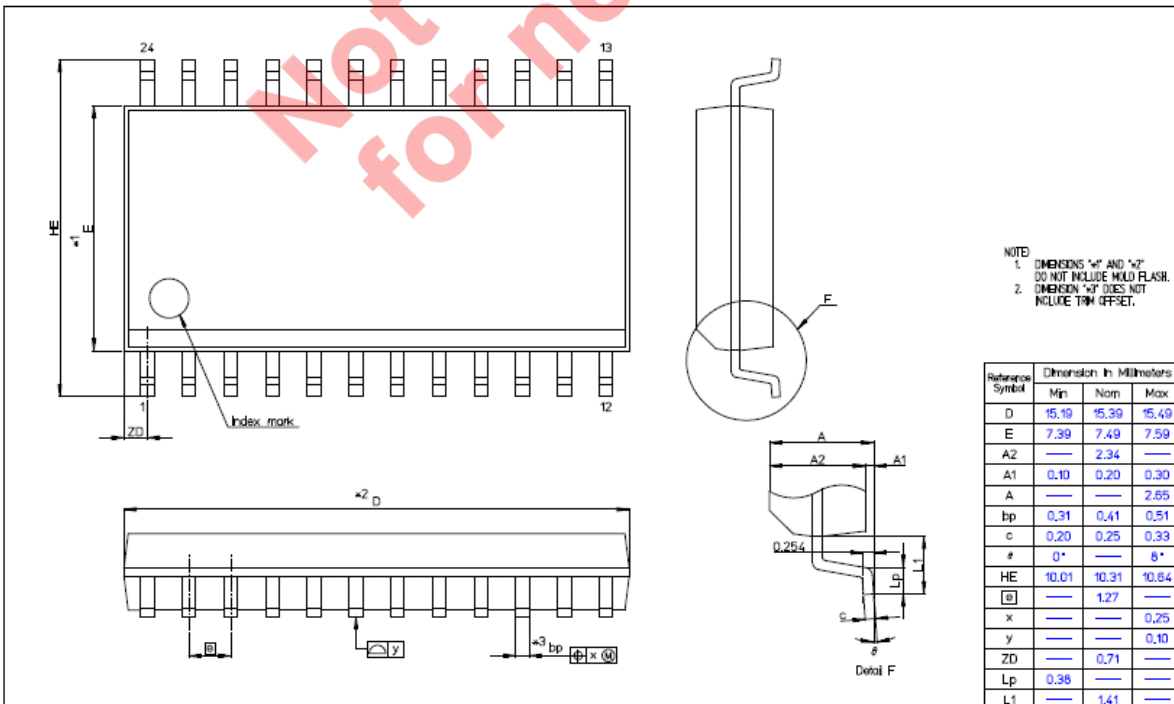
RENESAS

R8A66167SP   PRSP0036GC-A

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.79
A1	0.203	0.305	0.406
A2	—	2.286	—
D	15.748	15.875	16.002
E	7.391	7.493	7.595
HE	10.033	10.312	10.668
b	0.30	—	0.45
c	0.127	—	0.254
e	—	0.8	—
x	—	—	0.25
y	—	—	0.1
θ	0°	—	8°
ZD	—	1.137	—
Lp	0.508	0.762	1.016
L1	—	1.425	—
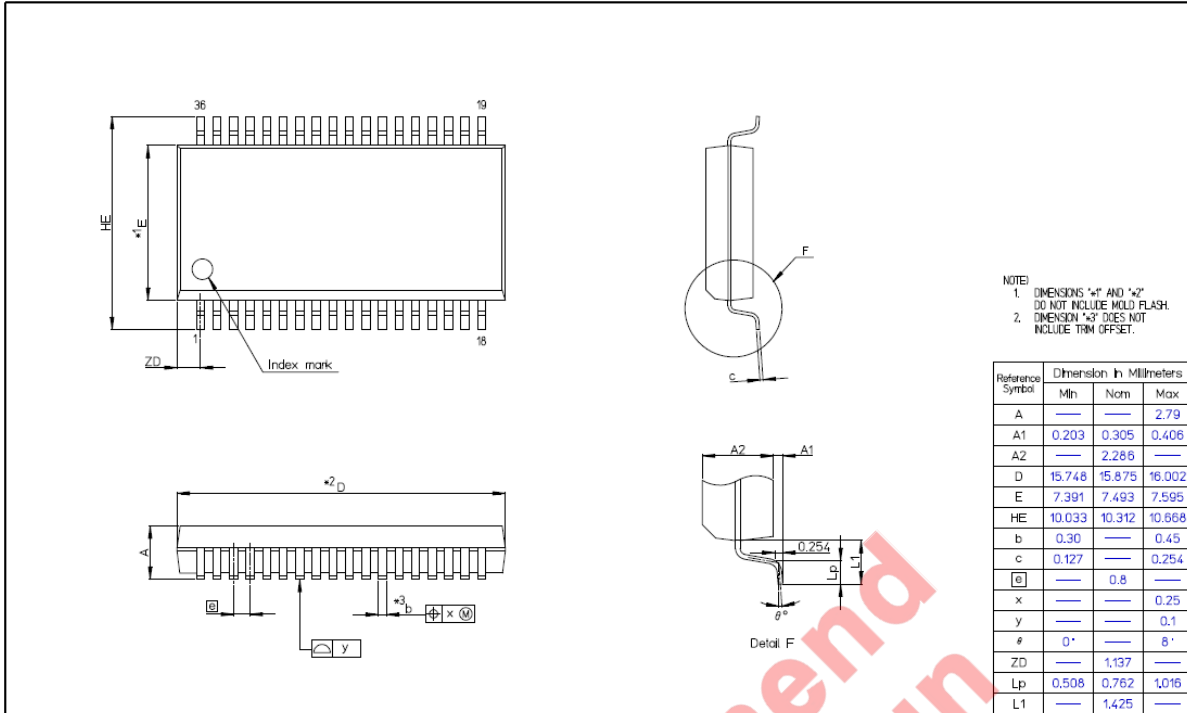
R8A66168SP   PRSP0048ZB-A

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.75	15.875	16.00
E	7.39	7.49	7.59
A2	—	2.29	—
A1	0.20	0.305	0.41
A	—	—	2.79
bp	0.20	0.27	0.34
c	0.127	0.22	0.254
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	0.635	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.635	—
Lp	0.50	0.76	1.02
L1	—	1.41	—
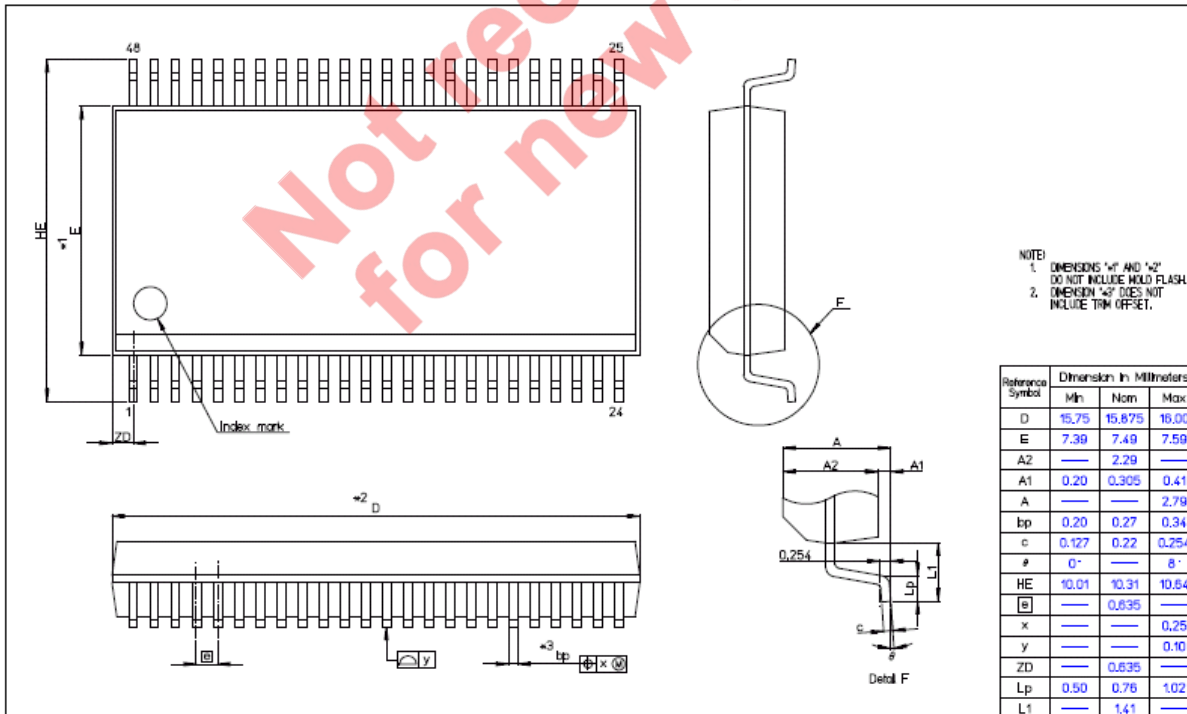
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Renesas Technology Corp.
Sales Strategic Planning Div.   Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510