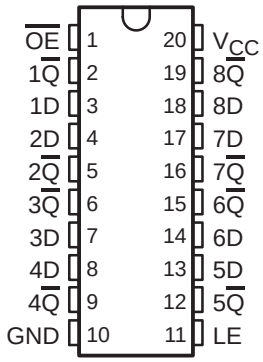
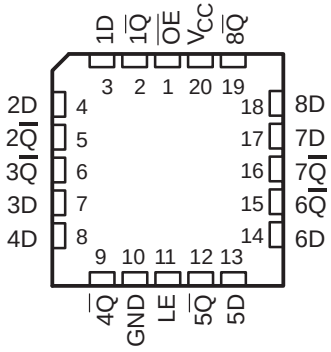
- **Inputs Are TTL-Voltage Compatible**
- **3-State Inverting Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54ACT533 . . . J OR W PACKAGE
SN74ACT533 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT533 . . . FK PACKAGE
(TOP VIEW)



description

The ’ACT533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverted levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT533 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT533 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

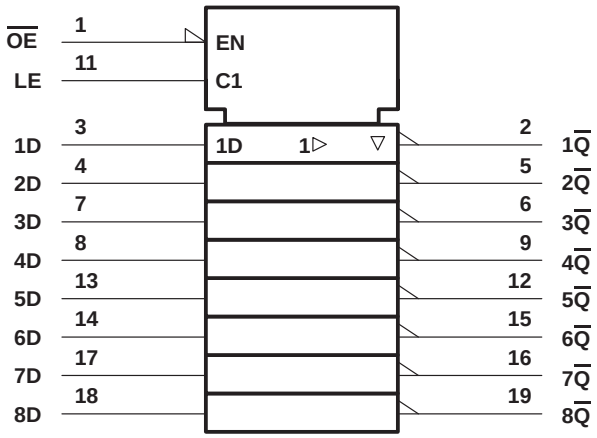
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

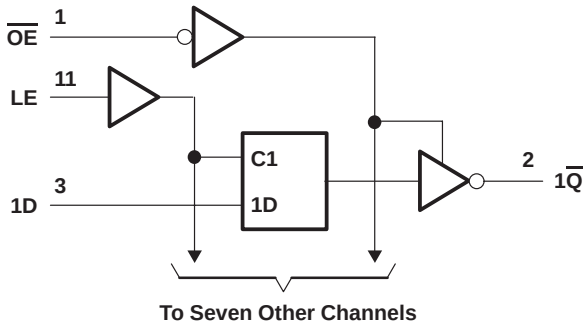
Copyright © 2000, Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54ACT533		SN74ACT533		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54ACT533		SN74ACT533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I_{OH} = –24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I_{OH} = –50 mA†	5.5 V				3.85				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.6		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54ACT533		SN74ACT533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		7.5		6		ns
t_{su}	Setup time, data before LE↓	3		5.5		4		ns
t_h	Hold time, data after LE↓	2		4		2.5		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C		SN54ACT533		SN74ACT533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	2.5	10.5	1.5	13	2	11.5	ns
t_{PHL}			2.5	10	1.5	12.5	2	11	
t_{PLH}	LE	$\overline{Q}$	2.5	10.5	1.5	13	2	11.5	ns
t_{PHL}			2.5	10.5	1.5	13	2	11.5	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
t_{PZL}			2	10	1	12.5	1.5	11	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
t_{PLZ}			2	10	1	12.5	1.5	11	

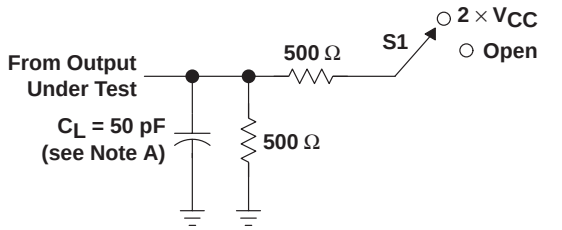
PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	40	pF

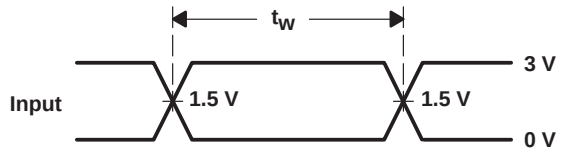
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

PARAMETER MEASUREMENT INFORMATION

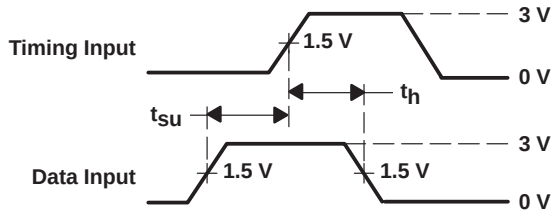


LOAD CIRCUIT

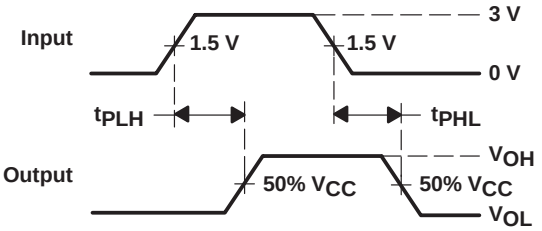
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open



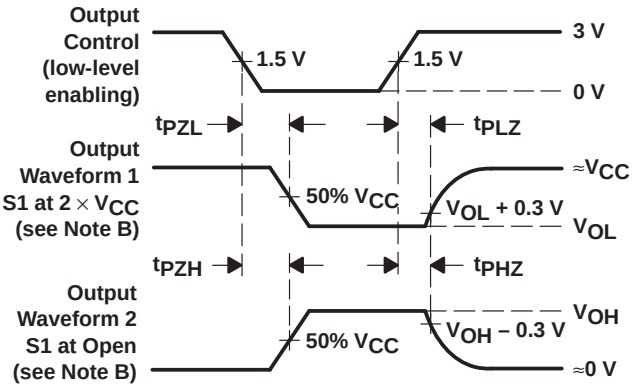
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated

SN74ACT533, Octal Transparent D-Type Latches With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ACT533
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	CMOS
Output Drive (mA)	-24/24
No. of Outputs	8
Static Current	0.04
th (ns)	2.5
tpd max (ns)	11.5
tsu (ns)	4
Logic	Inv

FEATURES

Back to Top

- Inputs Are TTL-Voltage Compatible
- 3-State Inverting Outputs Drive Bus Lines Directly
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-um Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

EPIC is a trademark of Texas Instruments Incorporated.

DESCRIPTION

Back to Top

The 'ACT533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the Q\ outputs follow the complements of the data (D) inputs. When LE is taken low, the Q\ outputs are latched at the inverted levels set up at the D inputs.

A buffered output-enable (OE\) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE\ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT533 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ACT533 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn74act533.pdf (98 KB,Rev.B) (Updated: 01/17/2000)

APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

Back to Top

View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ACT533DBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT533DW	SOP (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT533N	PDIP (N)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT533PWR	TSSOP (PW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

Back to Top

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74ACT533DBLE	OBSOLETE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74ACT533DBR	ACTIVE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU | 0.49	2000	N/A*	>10k | 07 Oct	8 WKS			
								>10k | 14 Oct				
SN74ACT533DW	ACTIVE	SOP (DW) | 20	-40 TO 85	View Contents	1KU | 0.49	25	1275	>10k | 07 Oct	8 WKS			
								>10k | 14 Oct				
SN74ACT533DWR	ACTIVE	SOP (DW) | 20	-40 TO 85	View Contents	1KU | 0.49	2000	N/A*	507 | 25 Sep	8 WKS			
								>10k | 04 Oct				

								>10k | 11 Oct					
SN74ACT533N	ACTIVE	PDIP (N) | 20	-40 TO 85	View Contents	1KU | 0.49	20	140	11 | 25 Sep	8 WKS	Avnet | AMERICA	130	BUY NOW
								>10k | 07 Oct					
								>10k | 14 Oct					
								>10k | 21 Oct					
SN74ACT533NSR	ACTIVE	SOP (NS) | 20		View Contents	1KU | 0.49	2000	N/A*	>10k | 07 Oct	8 WKS			
								>10k | 14 Oct					
SN74ACT533PWLE	OBSOLETE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74ACT533PWR	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.49	2000	N/A*	607 | 25 Sep	8 WKS			
								>10k | 03 Oct					
								>10k | 10 Oct					

Table Data Updated on: 9/26/2002

Texas Instruments © Copyright 1995-2002 Texas Instruments Incorporated. All rights reserved.
Trademarks | Privacy Policy | Terms of Use