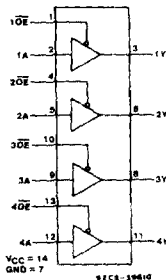


CD54/74HC125 CD54/74HCT125

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Buffer, 3-State

Type Features:

- Separate output enable inputs
- 3-state outputs

The RCA-CD54/74HC125 and CD54/74HCT125 contain 4 independent 3-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.

The CD54HC125 and CD54HCT125 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC125 and CD74HCT125 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- *Wide Operating Temperature Range:*
CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , @ $V_{CC} = 5 V$
- *CD54HCT/CD74HCT Types:*
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility $I_i \leq 1 \mu A$ @ V_{OL}, V_{OH}

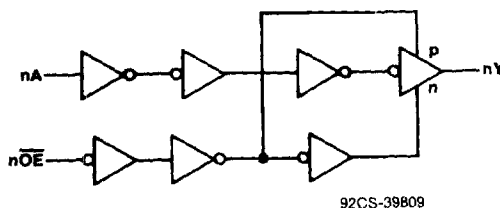


Fig. 1 - Logic diagram.

TRUTH TABLE

Inputs		Outputs
nA	nOE	nY
H	L	H
L	L	L
X	H	Z

- H = High Level
- L = Low Level
- X = Don't Care
- Z = High Impedance, OFF State

CD54/74HC125 CD54/74HCT125

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ± 20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ± 35 mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ± 70 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H) 500 mW

For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW

For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) 400 mW

For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to $+125^\circ\text{C}$

PACKAGE TYPE E, M -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

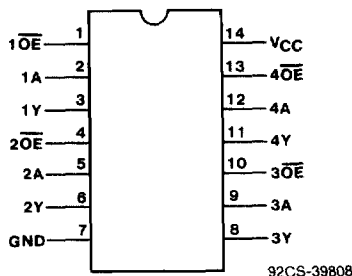
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) V_{CC} .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A : CD74 Types CD54 Types	-40 -55	+85 +125	$^\circ\text{C}$
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-39808
TERMINAL ASSIGNMENT

CD54/74HC125 CD54/74HCT125

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC125/CD54HC125										CD74HCT125/CD54HCT125										UNITS									
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE												
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C												
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max											
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5								V										
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—											
			6	4.2	—	—	4.2	—	4.2	—	—	5.5																		
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5								V										
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	—										
			6	—	—	1.8	—	1.8	—	1.8	—	5.5																		
High-Level Output Voltage V _{OH}	V _{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	V										
or	V _{IH}		4.5	4.4	—	—	4.4	—	4.4	—	or										4.5	4.4	—	—	4.4	—	4.4	—		
CMOS Loads	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}																			
TTL Loads (Bus Driver)	V _{IL}									V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V											
or	V _{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—										or	4.5	3.98	—	—	3.84	—	3.7	—		
	V _{IH}	-7.8	6	5.48	—	—	5.34	—	5.2	—										V _{IH}										
Low-Level Output Voltage V _{OL}	V _{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V										
or	V _{IH}		4.5	—	—	0.1	—	0.1	—	0.1	—										or	4.5	—	—	0.1	—	0.1	—	0.1	
CMOS Loads	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	—										V _{IH}									
TTL Loads (Bus Driver)	V _{IL}									V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	V											
or	V _{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4										or	4.5	—	—	0.26	—	0.33	—	0.4		
	V _{IH}	7.8	6	—	—	0.26	—	0.33	—	0.4										V _{IH}										
Input Leakage Current I _I	V _{CC}		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA										
or	Gnd																													
Quiescent Device Current I _{CC}	V _{CC}	0	6	—	—	8	—	80	—	160	V _{CC}	5.5	—	—	8	—	80	—	160	μA										
or	Gnd																				or	5.5	—	—	8	—	80	—	160	
Additional Quiescent Current per Input Pin: 1 Unit Load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA										
3-State Leakage Current I _{OZ}	V _{IL} or V _{IH}	V _O =V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA										

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
nA, nOE	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC125 CD54/74HCT125

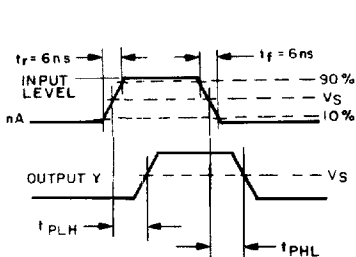
SWITCHING CHARACTERISTICS ($V_{CC}=5\text{ V}$, $T_A=25^\circ\text{C}$, Input $t_r=6\text{ ns}$)

CHARACTERISTIC	C_L pF	TYPICAL		UNITS
		HC	HCT	
Propagation Delay Time: (Fig. 2) nA to nY	t_{PLH} t_{PLH}	15	8 10	ns
Output Enabling Time	t_{PZL} , t_{PZH}	15	10 10	
Output Disabling Time	t_{PLZ} , t_{PHZ}	15	10 11	
Power Dissipation Capacitance*	C_{PD}	—	29 34	pF

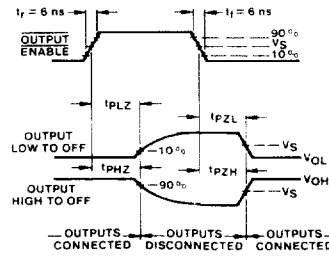
* C_{PD} is used to determine the dynamic power consumption, per channel. $P_D=V_{CC}^2 f_i (C_{PD}+C_L)$ where: f_i =input frequency
 C_L =load capacitance
 V_{CC} =supply voltage

SWITCHING CHARACTERISTICS ($C_L=50\text{ pF}$, Input $t_r=6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC} V	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time nA to nY (Fig. 2)	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
	t_{PHL}	4.5	—	20	—	25	—	25	—	31	—	30	—	38	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Enable Delay Time (Fig. 2)	t_{PZH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
	t_{PZL}	4.5	—	25	—	25	—	31	—	31	—	38	—	38	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Disable Delay Time	t_{PHZ} , t_{PLZ}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
		4.5	—	25	—	28	—	31	—	35	—	38	—	42	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition Time	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_i	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_o	—	—	20	—	20	—	20	—	20	—	20	—	20	



92CS-3853IRI



92CS-39806

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Transition and propagation delay times.

CD54/74HC125 CD54/74HCT125

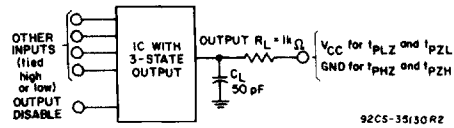


Fig. 3 - Three-state propagation delay test circuit.