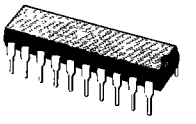
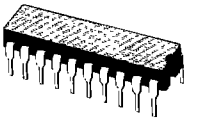
# QUAD 2-PORT REGISTER

- FULLY POSITIVE EDGE-TRIGGERED OPERATION
- SELECT FROM TWO DATA SOURCES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



**B1**
(Plastic Package)



**D1**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

T74LS399 D1
T74LS399 B1
T74LS399 C1
T74LS399 M1

## DESCRIPTION

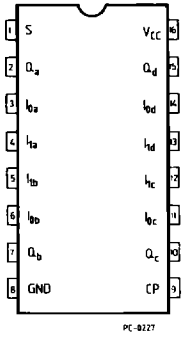
The T74LS399 is a Quad 2-Port Register. It is logical equivalent to a quad 2-input multiplexer followed by a 4-bit edge-triggered register. The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input.

## PIN NAMES

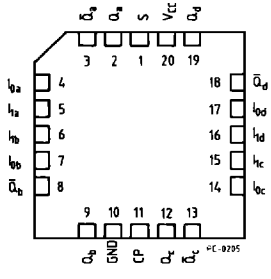
| | |
|---|---|
| S | COMMON SELECT INPUT |
| CP | CLOCK (Active HIGH going edge) INPUT |
| $I_{0a}$–$I_{0d}$ | DATA INPUT FROM SOURCE 0 |
| $I_{1a}$–$I_{1d}$ | DATA INPUT FROM SOURCE 1 |
| $Q_a$–$Q_d$ | REGISTER TRUE OUTPUTS |
| $\overline{Q}_a$–$\overline{Q}_d$ | REGISTER COMPLEMENTARY OUTPUTS |

## PIN CONNECTION (top view)

DUAL IN LINE




CHIP CARRIER




NC = No Internal Connection

## FUNCTIONNAL DESCRIPTION

This high speed Quad 2-Port Register selects four bits of data from two sources (Port) under the control of a Common Select Input (S). The 4-bit Output Register where selected data are transferred is synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit RS type output register is fully edge-triggered. Predictable operation is assured if Data inputs (I) and select inputs (S) are kept stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input.

## TRUTH TABLE

| Inputs | | | Outputs |
|---|---|---|---|
| S | $I_0$ | $I_1$ | Q |
| l | l | X | L |
| l | h | X | H |
| h | X | l | L |
| h | X | h | H |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't care
l = LOW Voltage Level one set-up Time Prior to the LOW-to-HIGH Clock Transition
h = High Voltage Level one set-up Time Prior to the LOW-to-HIGH Clock Transition

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | – 0.5 to 7 | V |
| $V_I$ | Input Voltage, Applied to Input | – 0.5 to 15 | V |
| $V_O$ | Output Voltage, Applied to Output | 0 to 10 | V |
| $I_I$ | Input Current, Into Inputs | – 30 to 5 | mA |
| $I_O$ | Output Current, Into Outputs | 50 | mA |

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGE

| Part Numbers | Supply Voltage | | | Temperature |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| T74LS399XX | 4.75 V | 5.0 V | 5.25 V | 0 °C to + 70 °C |

XX = package type.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Symbol | Parameter | Limits | | | Test Condition (note 1) | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. (*) | Max. | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | Guaranteed Input HIGH Voltage for all Inputs | | V |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | Guaranteed Input LOW Voltage for all Inputs | | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | - 0.65 | - 1.5 | $V_{CC}$ = MIN, $I_{IN}$ = -18 mA | | V |
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.4 | | $V_{CC}$ = MIN, $I_{OH}$ = - 400 µA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | | V |
| $V_{OL}$ | Output LOW Voltage | | 0.25 | 0.4 | $I_{OL}$ = 4.0 mA | $V_{CC}$ = MIN<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>per Truth Table | V |
| | | | 0.35 | 0.5 | $I_{OL}$ = 8.0 mA | | V |
| $I_{IH}$ | Input HIGH Current | | | 20<br>40 | $V_{CC}$ = MAX. $V_{IN}$ = 2.7 V<br>$V_{CC}$ = MAX. $V_{IN}$ = 7.0 V | | µA<br>mA |
| $I_{IL}$ | Input LOW Current | | | - 0.4 | $V_{CC}$ = MAX. $V_{IN}$ = 0.4 V | | mA |
| $I_{OS}$ | Output Short Circuit Current (note 2) | - 20 | | - 100 | $V_{CC}$ = MAX. $V_{OUT}$ = 0 V | | mA |
| $I_{CC}$ | Supply Current | | | 13 | $V_{CC}$ = MAX | | mA |

**Notes :** 1 For conditions shown as MIN or MAX, use the appropriate value specified under garanteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = 25 °C.

## AC CHARACTERISTICS : $T_A$ = 25 °C

| Symbol | Parameter | Limits | | | Test Conditions | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Clock to Output Q | | 18<br>21 | 27<br>32 | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF | ns |

## AC SET-UP REQUIREMENTS : $T_A$ = 25 °C

| Symbol | Parameter | Limits | | | Test Conditions | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $t_W$ | Clock Pulse Width | 20 | | | $V_{CC}$ = 5.0 V | ns |
| $t_s$ | Data Set-up Time | 25 | | | | ns |
| $t_s$ | Select Set-up Time | 45 | | | | ns |
| $t_h$ | Hold Time, Any Input | 0 | | | | ns |

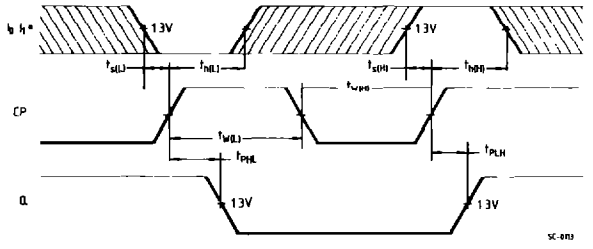
### DEFINITION OF TERMS

SET-UP TIME ($t_s$) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME ($t_h$) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

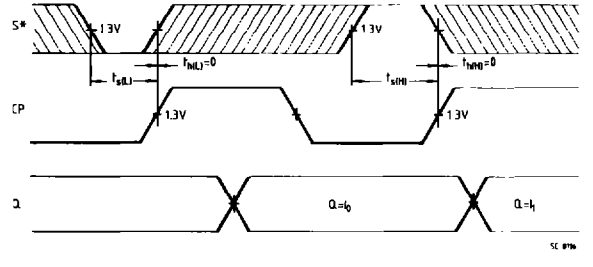
## AC WAVEFORMS

### Figure 1 .




* The shaded areas indicate when the input is permitted to change for predictable output performance.

### Figure 2 .




* The shaded areas indicate when the input is permitted to change for predictable output performance.

### Figure 3 .