National Semiconductor

ADVANCE INFORMATION

74ABT823
9-Bit D-Type Flip-Flop with TRI-STATE® Outputs

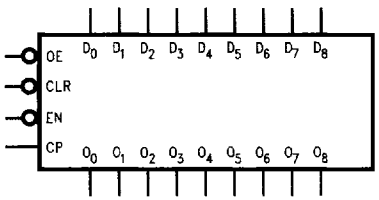
General Description

The 'ABT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

Features

- TRI-STATE outputs
- Clock Enable and Clear
- Guaranteed latch up protection
- Non-destructive hot insertion capability
- High impedance glitch free bus loading during entire power up and power down cycle

Logic Symbols



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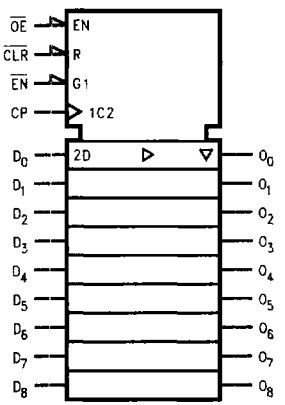
IEEE/IEC



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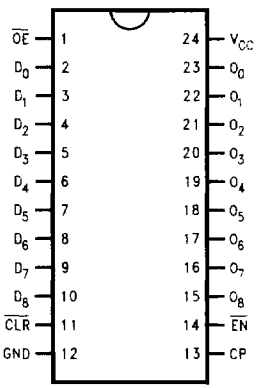
Connection Diagram

Pin Assignment for SOIC



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Functional Description

The 'ABT823 device consists of nine D-type edge-triggered flip-flops. It has TRI-STATE true outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 'ABT823 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins.

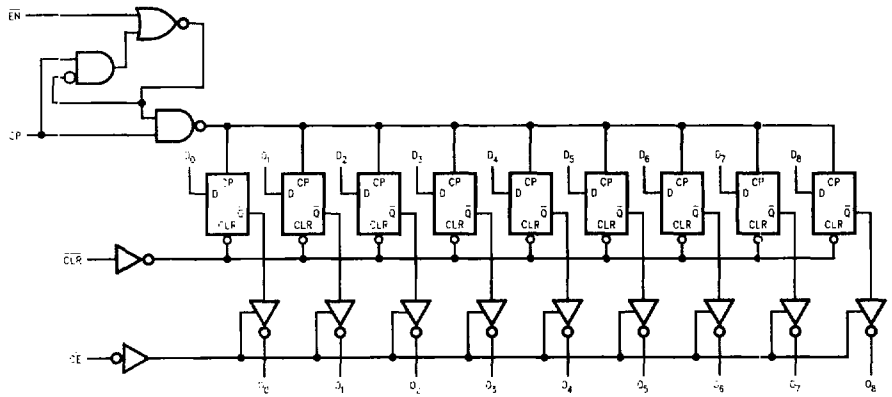
When the $\overline{CLR}$ is LOW and the $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW to HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	↗	H	H	Z	Load
H	H	L	↗	H	L	Z	Load
L	H	L	↗	L	H	L	Data Available
L	H	L	↗	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.