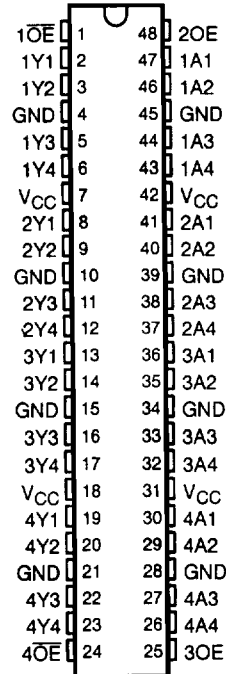


**SN74LVC16241**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

**DGG OR DL PACKAGE**  
(TOP VIEW)



**description**

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation; it can interface to a 5-V system environment.

The SN74LVC16241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-enable (OE and  $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16241 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**PRODUCT PREVIEW**

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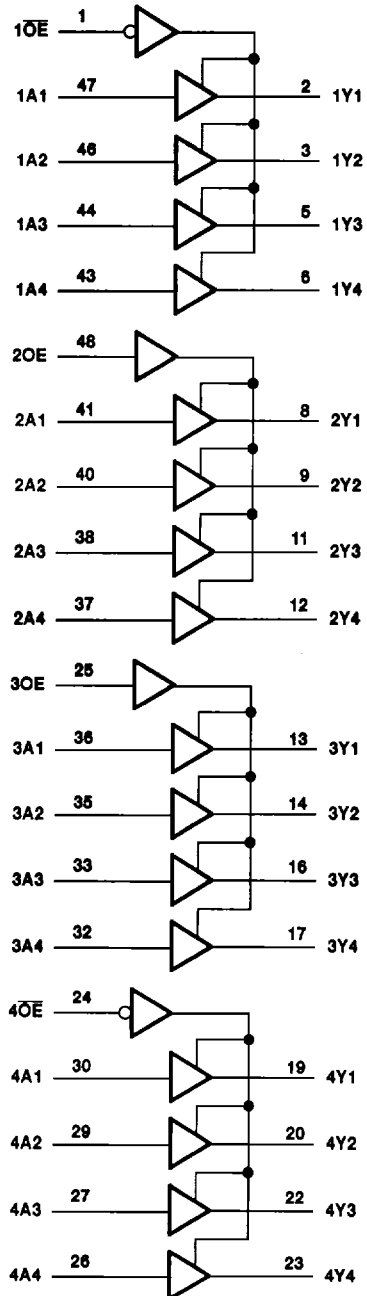
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**FUNCTION TABLES**

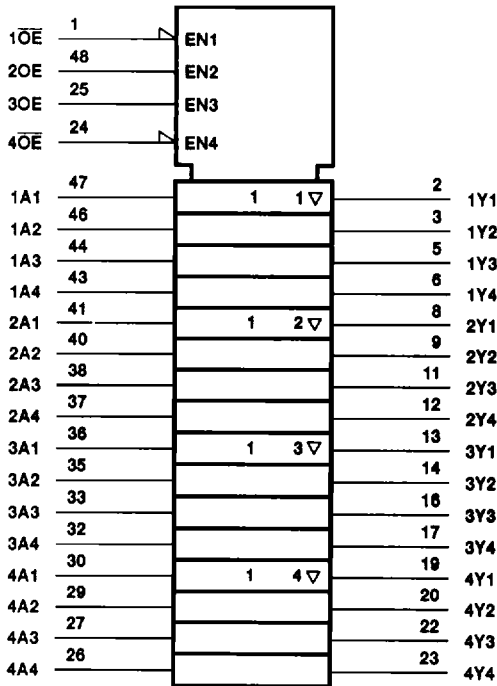
INPUTS		OUTPUTS
1OE, 4OE	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

**logic diagram (positive logic)**



**logic symbol†**



**PRODUCT PREVIEW**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	0.85 W
DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating		V
		2	3.6	
		Data retention only		
		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

**PRODUCT PREVIEW**



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> †	MIN	TYP‡	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 µA	MIN to MAX	V <sub>CC</sub> -0.2			V
		I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		I <sub>OH</sub> = -24 mA	3 V	2.4			
		I <sub>OH</sub> = -24 mA	3 V	2.2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	MIN to MAX			0.2	V
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>		V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	µA
I <sub>I</sub> (hold)	Data inputs	V <sub>I</sub> = 0.8 V	3 V		75		µA
		V <sub>I</sub> = 2 V			-75		
I <sub>OZ</sub>		V <sub>O</sub> = 5.5 V or GND	3.6 V			±10	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	µA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ All typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

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