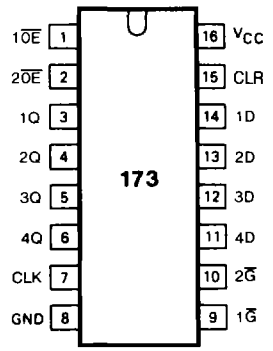
GD54/74HC173, GD54/74HCT173
QUAD 3-STATE D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

General Description

These devices are identical in pinout to the 54/74LS173. They consist of four D-type flip-flops operating synchronously from a common Clock and clear. Data, when enabled, are clocked into the four D-type flip-flops on the rising edge of the common clock. When either or both of the output enable controls is high, the outputs are in a high-impedance state. The clear feature is asynchronous and active-high. These deveices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	$\overline{CLR}$	CLK	1$\overline{G}$	2$\overline{G}$	nD	nQ (register)
clear	H	X	X	X	X	L
parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	nQ (register)	1$\overline{OE}$	2$\overline{OE}$	1Q	2Q	3Q	4Q
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CLK transition
X = dont care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I<-0.5$ or $V_I>V_{CC}+0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V<V_O<V_{CC}+0.5V$		|35|	mA
I_{CC}	DC V_{CC} or GND current			|70|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C. derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX	
Supply-Voltage Range V_{CC}: GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5 5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f GD54/74HC Types at 2V		1000	ns
at 4 5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

Logic Diagram

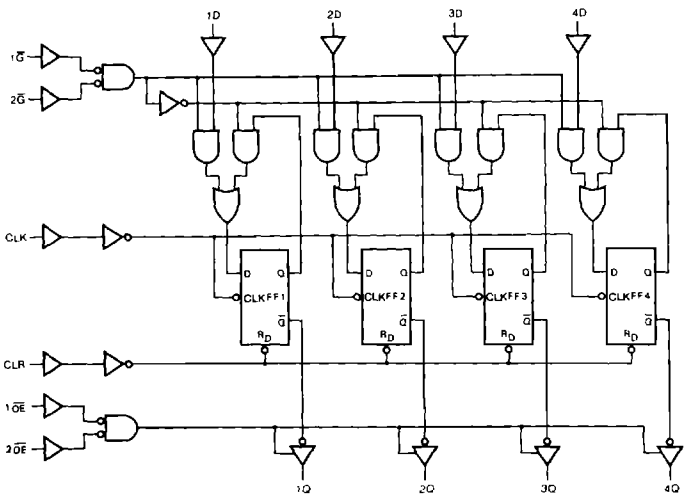


Fig. 1 Logic symbol

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC173		GD54HC173		UNIT
					MIN	TYP	MAX.	MIN	MAX	MIN	MAX.	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH}=-6mA$ $I_{OH}=-7.8mA$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			$I_{OL}=6mA$ $I_{OL}=7.8mA$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		6.0			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN}=V_{IH}$ or V_{IL}	$V_O=V_{CC}$ or GND	6.0		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT173		GD54HCT173		UNIT
					MIN	TYP.	MAX	MIN.	MAX.	MIN.	MAX	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5		4.4		4.4		V
			$I_{OH}=-6mA$	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5			0.1		0.1		0.1	V
			$I_{OL}=6mA$	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		5.5			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN}=V_{IH}$ or V_{IL}	$V_O=V_{CC}$ or GND	5.5		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		5.5		0.01	8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC173		GD54HC173		UNIT
				MIN.	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse width	$\overline{CLR}$	2 0	80	30		100		120		ns
			4.5	16	10		20		25		
			6 0	14	8		18		22		
		CLK	2 0	80	30		100		120		ns
			4 5	16	10		20		25		
			6 0	14	8		18		22		
t_{su}	Set up time before CLK ↑	Data to CLK	2 0	60	30		80		100		ns
			4 5	15	10		18		20		
			6 0	14	8		16		18		
		$\overline{PR}$ or $\overline{CLR}$ to CLk	2 0	5	0		5		5		ns
			4 5	5	0		5		5		
			6 0	5	0		5		5		
t_h	Hold time	CLK to Data	2 0	3	0		3		3		ns
			4 5	3	0		3		3		
			6 0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HC173		GD54HC173		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2 0	6	20		5		4		MHz
		4 5	30	65		25		20		
		6.0	35	75		30		25		
t_{PLH} t_{PHL}	Propagation Delay time CLK to nQ	2 0		65	170		220		300	ns
		4 5		17	34		42		55	
		6 0		16	32		38		50	
t_{PLH} t_{PHL}	Propagation Delay time $\overline{CLR}$ to nQ	2 0		55	160		210		260	ns
		4.5		16	32		40		50	
		6.0		15	26		32		38	
t_{PZH} t_{PZL}	3-state Output Enable Time n$\overline{OE}$ to nQ	2 0		50	150		190		230	ns
		4 5		16	30		38		45	
		6 0		15	26		32		38	
t_{PHZ} t_{PLZ}	3-state Output Disable Time n$\overline{OE}$ to nQ	2 0		50	150		190		220	ns
		4 5		16	30		38		45	
		6 8		15	26		32		38	
t_{TLH} $t2_{THL}$	Output Transition time	2 0		15	60		75		90	ns
		4 5		6	12		15		22	
		6.0		6	13		13		12	

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC}	$T_A=25°C$			GD74HCT173		GD54HCT173		UNIT
				MIN.	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse width	$\overline{CLR}$	4.5	18	10		20		25		ns
		CLK	4.5	10	10		20		25		ns
t_{su}	Setup time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{PR}$ or $\overline{CLR}$ to CLK	4.5	5	0		5		5		ns
t_h	Hold time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC}	$T_A=25°C$			GD74HCT173		GD54HCT173		UNIT
			MIN	TYP	MAX.	MIN	MAX.	MIN.	MAX	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay time CLK to nQ	4.5		18	36		44		56	ns
t_{PLH} / t_{PHL}	Propagation Delay time $\overline{CLR}$ to nQ	4.5		17	34		42		52	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time n$\overline{OE}$ to nQ	4.5		17	32		40		40	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time n$\overline{OE}$ to nQ	4.5		17	32		40		40	ns
t_{TLH} / t_{THL}	Output Transition time	4.5		7	12		15		18	ns

AC Waveforms

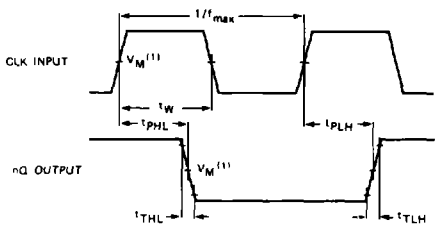


Fig. 2 Waveforms showing the clock (CLK) to output (nQ) propagation delays, the clock pulse width, the output transition times and the meximum clock pulse frequency.

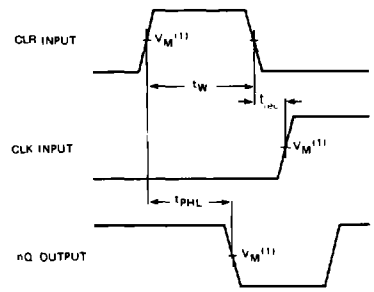


Fig. 3 Waveforms showing the master clear (CLR) pulse width, the master clear to output (nQ) propagation delays and the master clear to clock (CLK) recovery time.

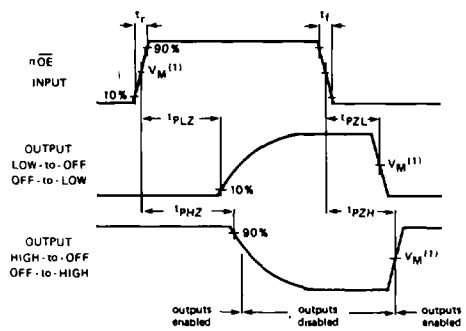


Fig. 4 Waveforms showing the 3-state enable and disable times.

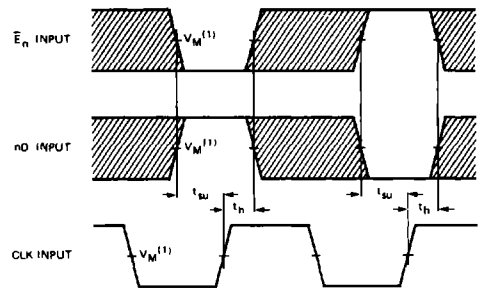


Fig. 5 Waveforms showing the data set-up and hold times from input (nG, nD) to clock (CLK).

Note to Fig. 5
The shaded areas indicate when the input is permitted to change for predictable output performance

Note to AC waveforms

For HC V_M = 50%, V_I = GND to V_{CC}
HCT V_M = 1.3V, V_I = GND to 3V