



CYPRESS

CY29FCT52T

## 8-Bit Registered Transceiver

### Features

- Function, pinout, and drive compatible with FCT, F Logic and AM2952
- FCT-C speed at 6.3 ns max. (Com'1)  
FCT-B speed at 7.5 ns max. (Com'1)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- ESD > 2000V

- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink Current      64 mA (Com'1),  
48 mA (Mil)
- Source Current    32 mA (Com'1),  
12 mA (Mil)

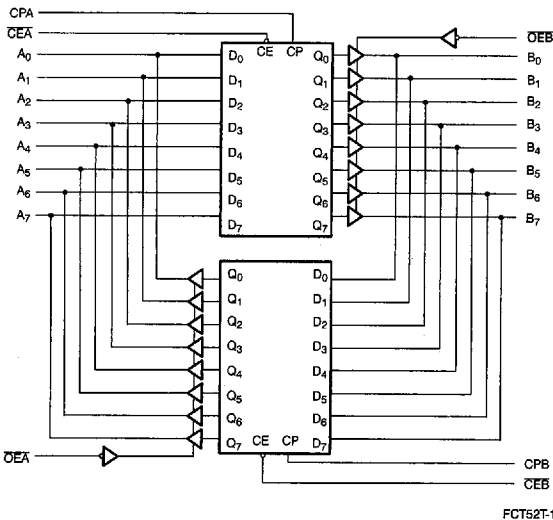
both directions between two bidirectional buses. Separate clock, clock enable, and three-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64 mA.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

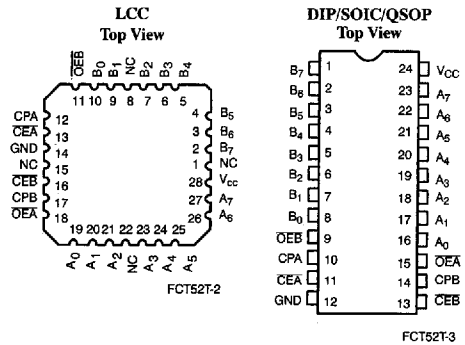
### Functional Description

The CY29FCT52T has two 8-bit back-to-back registers that store data flowing in

### Logic Block Diagram



### Pin Configurations



### Function Table<sup>[1]</sup>

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	$\uparrow$	L	L	Load Data
H	$\uparrow$	L	H	Load Data

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

### Output Control

$\overline{OE}$	Internal Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	Enable Outputs

**Pin Description**

Name	Description
A	A register inputs or B register outputs.
B	B register inputs or A register outputs.
CPA	Clock for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	Clock Enable for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A register holds its contents regardless of CPA signal transitions.
$\overline{OEA}$	Output Enable for the A register. When $\overline{OEA}$ is LOW, the A register outputs are enabled onto the B lines. When $\overline{OEA}$ is HIGH, the B outputs are in the high impedance state.
CPB	Clock for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	Clock Enable for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B register holds its contents regardless of CPA signal transitions.
$\overline{OEB}$	Output Enable for the B register. When $\overline{OEB}$ is LOW, the B register outputs are enabled onto the A lines. When $\overline{OEB}$ is HIGH, the A outputs are in the high impedance state.

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

**Notes:**

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

- T<sub>A</sub> is the "instant on" case temperature.

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions		Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> = -32 mA	Com'1	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> = -15 mA	Com'1	2.4	3.3		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> = -12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'1		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =48mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> = -18 mA			-0.7	-1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V				±1	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V		-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V				±1	μA

**Capacitance<sup>[6]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

5. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>= +25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.1	0.2	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V, <sup>[8]</sup> f <sub>1</sub> =0, Outputs Open	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OEA or OEB=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.06	0.12	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, OEA or OEB=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.7	1.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, OEA or OEB=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.2	3.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, OEA or OEB=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	1.6	3.2 <sup>[11]</sup>	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, OEA or OEB=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	3.9	12.2 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.  
 9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.  
 10. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>1</sub>)  
 I<sub>CC</sub> = Quiescent Current with CMOS input levels  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL inputs HIGH

- N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
 f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
 f<sub>1</sub> = Input signal frequency  
 N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

- All currents are in milliamps and all frequencies are in megahertz.  
 11. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

**Switching Characteristics Over the Operating Range**

Parameter	Description	29FCT52AT				29FCT52BT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial		Military		Commercial			
		Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CPA, CPB to A, B	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEA or OEB to A or B	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEA or OEB to A or B	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		2.5		2.5		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW, A, B to CPA, CPB	2.0		2.0		1.5		1.5		ns	4
t <sub>S</sub>	Set-Up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0		3.0		3.0		3.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0		2.0		2.0		2.0		ns	4
t <sub>w</sub>	Pulse Width, <sup>[6]</sup> HIGH or LOW, CPA or CPB	3.0		3.0		3.0		3.0		ns	5

Parameter	Description	29FCT52CT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial			
		Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CPA, CPB to A, B	2.0	7.3	2.0	6.3	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time, OEA or OEB to A or B	1.5	8.0	1.5	7.0	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time, OEA or OEB to A or B	1.5	7.5	1.5	6.5	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW, A, B to CPA, CPB	1.5		1.5		ns	4
t <sub>S</sub>	Set-Up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0		3.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0		2.0		ns	4
t <sub>w</sub>	Pulse Width, <sup>[6]</sup> HIGH or LOW, CPA or CPB	3.0		3.0		ns	5

**Notes:**

12. Minimum limits are guaranteed but not tested on Propagation Delays.  
 13. See "Parameter Measurement Information" in the General Information Section.

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY29FCT52CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY29FCT52CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY29FCT52BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY29FCT52BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY29FCT52ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY29FCT52ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52ATLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00262-A