FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT162H952AT/BT/CT/ET

FEATURES:

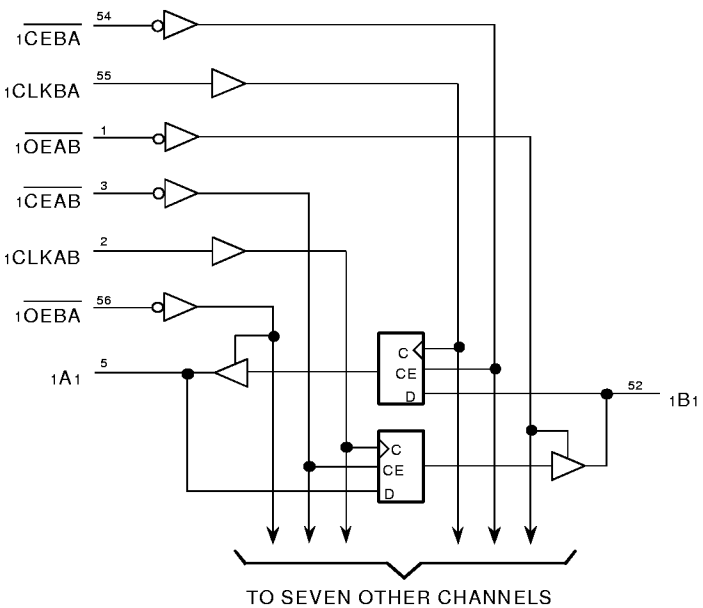
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage ≤ 1µA (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors

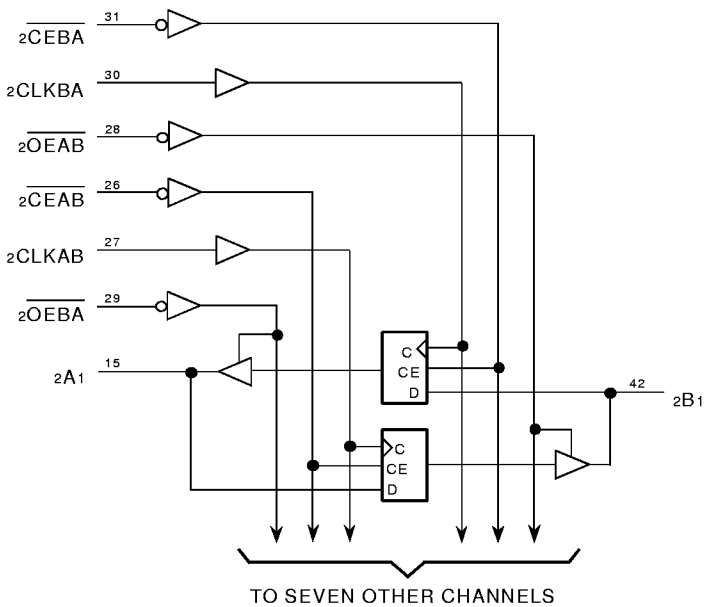
DESCRIPTION:

The FCT162H952AT/BT/CT/ET 16-bit registered transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $xOEAB$ performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using $xCEBA$, xCLKBA, and $xOEBA$ inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

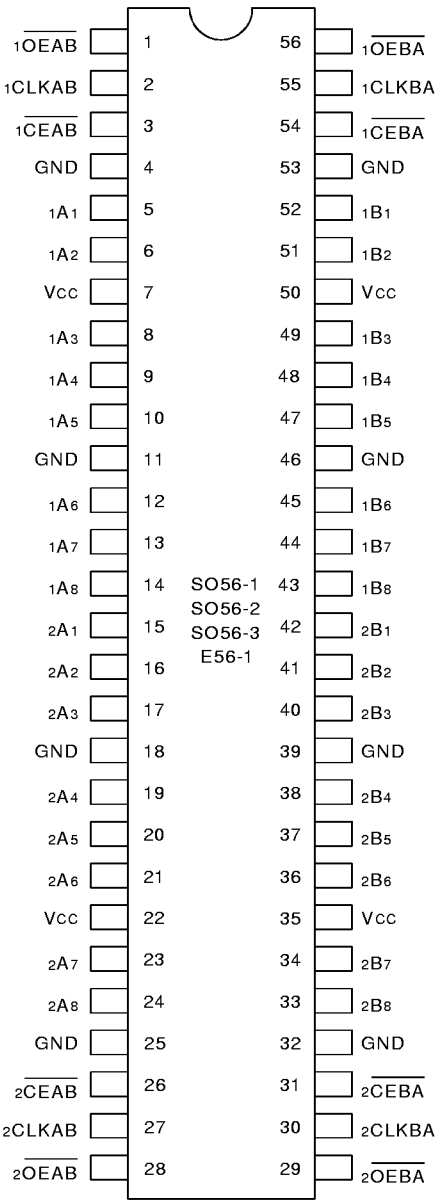
The FCT162H952AT/BT/CT/ET has "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs[1]
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs[1]

NOTE:
1. These pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE[1,3]

Inputs				Outputs
$x\overline{CEAB}$	xCLKAB	$x\overline{OEAB}$	xAx	xBx
H	X	L	X	B[2]
X	L	L	X	B[2]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:
1. A-to-B data flow is shown: B-to-A data flow is similar but uses $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS-HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{BHH} I_{BHL}	Bus-hold Sustain Current[4]	Bus-hold Input	V_{CC} = Min.	V_I = 2V	–50	—	—	µA
				V_I = 0.8V	50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5, 6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus-hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Does not include Bus-hold I/O pins.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L	—	0.3	0.55	V

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	20[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL

Symbol	Parameter	Condition[1]	FCT162H952AT		FCT162H952BT		FCT162H952CT		FCT162H952ET		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2	10	2	7.5	2	6.3	1.5	3.7	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	8	1.5	7	1.5	4.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10	1.5	7.5	1.5	6.5	1.5	3.6	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2	—	1.5	—	1.5	—	0	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3	—	3	—	3	—	2	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2	—	2	—	2	—	0	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3	—	3	—	3	—	3	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

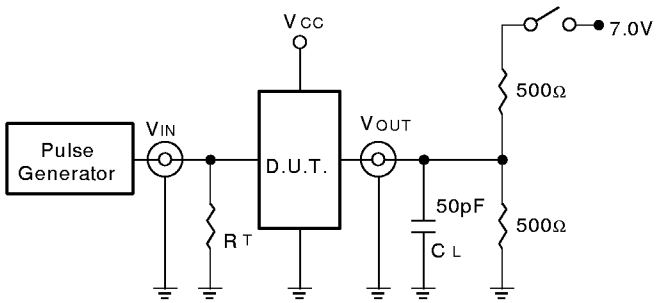
Symbol	Parameter	Condition[1]	FCT162H952AT		FCT162H952BT		FCT162H952CT		FCT162H952ET		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2	11	2	8	2	7.3	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	13	1.5	8.5	1.5	8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10	1.5	8	1.5	7.5	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	—	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2	—	1.5	—	1.5	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3	—	3	—	3	—	—	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2	—	2	—	2	—	—	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3	—	3	—	3	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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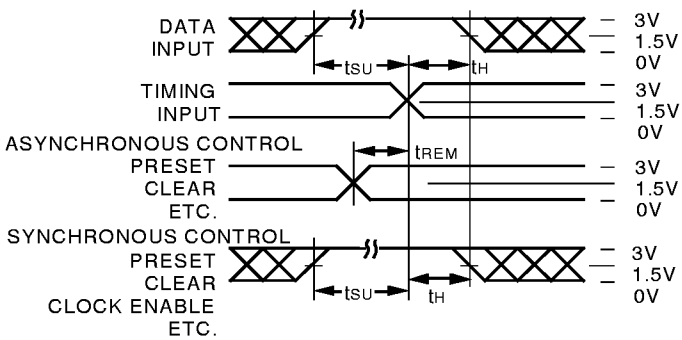
DEFINITIONS:

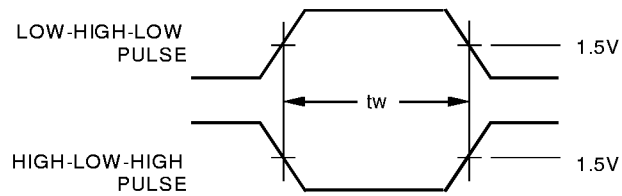
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



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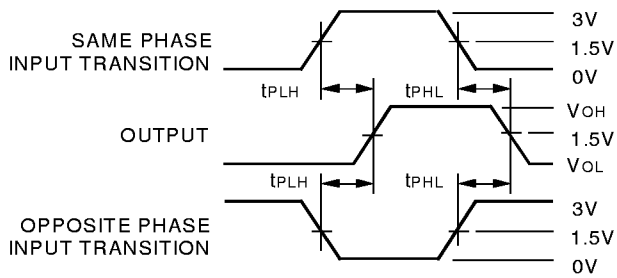
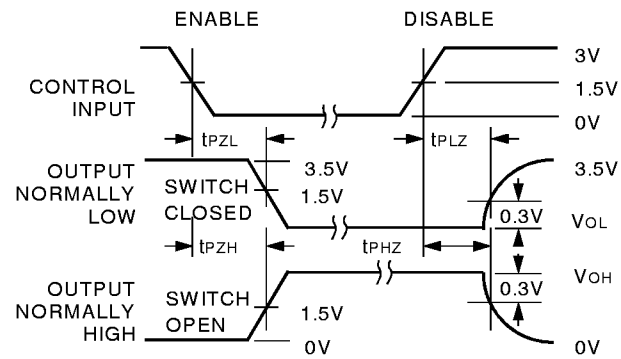


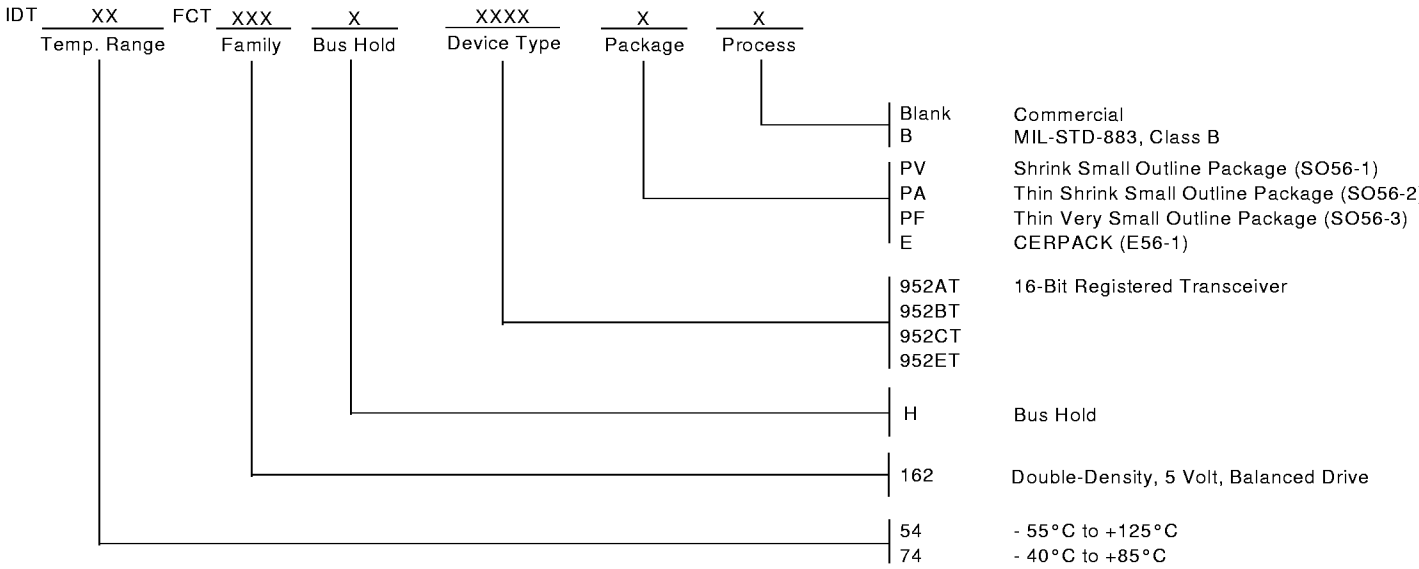
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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