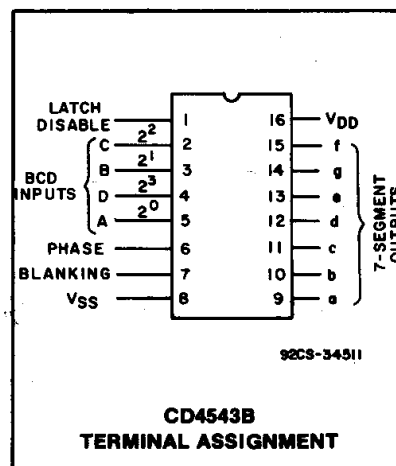


CMOS BCD-to-Seven-Segment Latch/Decoder/Driver For Liquid-Crystal Displays

High-Voltage Types (20-Volt Rating)

Features:

- Display blanking of all illegal input combinations
- Latch storage of code
- Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range
- Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})
- Direct LED driving capability



■ CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS}. It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

The CD4543B is supplied in hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
Voltages referenced to V _{SS} Terminal) -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ±10mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C 500mW
For T _A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T _A) -55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg}) -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD}=5 V
2 V at V_{DD}=10 V
2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Instrument display driver
- Dashboard display driver
- Computer/calculator display driver
- Timing device driver (clocks, watches, timers)

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4543B Types

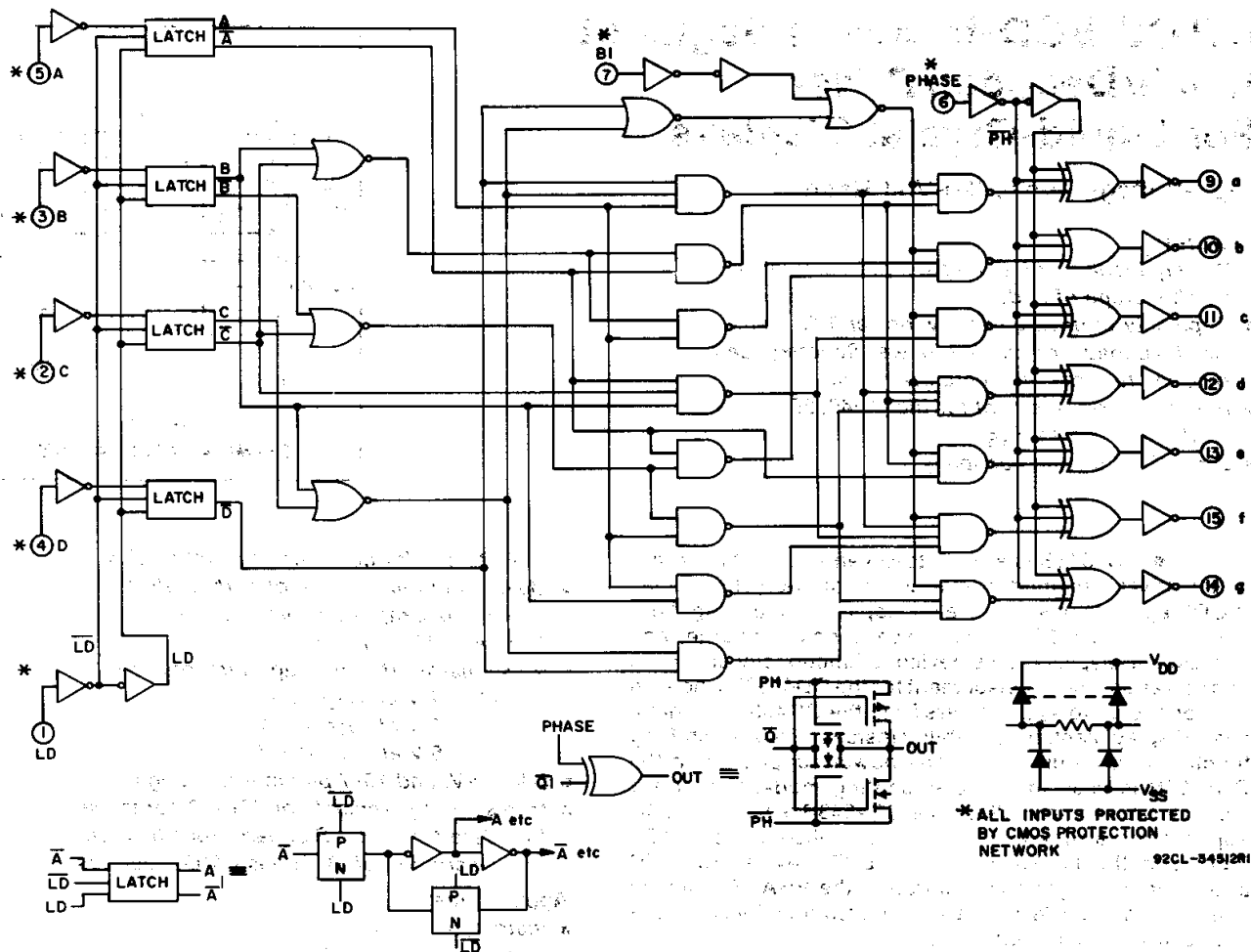


Fig. 1 - BCD-to-seven-segment latch/decoder/driver CD4543B logic circuit diagram.

RECOMMENDED OPERATING CONDITIONS at $T_A=25^\circ\text{C}$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range)	—	3	18	V
Latch Disable Pulse Width	5	250	125	ns
	10	100	50	
	15	80	40	
Minimum Data Setup Time	5	60	15	
	10	20	-5	
	15	10	-5	
Minimum Data Hold Time	5	25	-5	
	10	20	10	
	15	20	10	

CD4543B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current Max. I _{DD}	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current Min. I _{OL}	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I _{OH}	4.6	0, 5	5	-0.46	-0.44	-0.30	-0.26	-0.37	-0.75	—	mA
	2.5	0, 5	5	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	9.5	0,10	10	-0.98	-0.92	-0.68	-0.55	-0.8	-1.6	—	
	13.5	0,15	15	-3.33	-3.18	-2.2	-1.9	-2.7	-5.4	—	
Output Voltage: Low-Level Max. V _{OL}	—	0, 5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V _{OH}	—	0, 5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage Max. V _{IL}	0.5,4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min. V _{IH}	0.5,4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current Max. I _{IN}	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

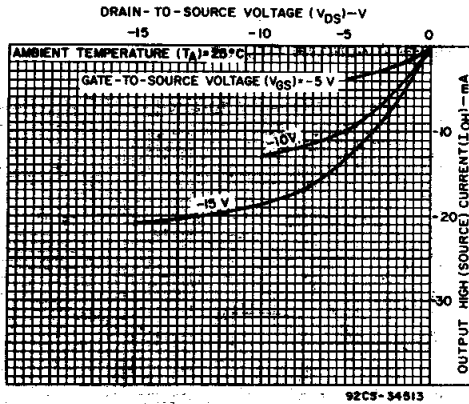


Fig. 2 - Typical output high (source) current characteristics.

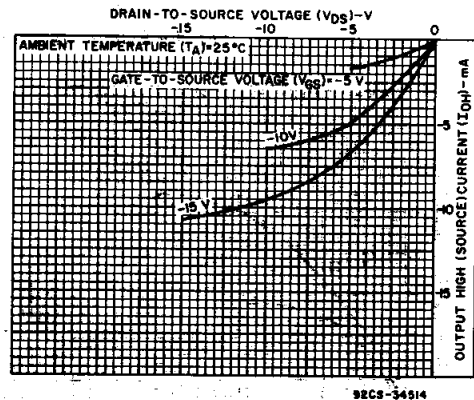


Fig. 3 - Minimum output high (source) current characteristics.

CD4543B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$; $C_L=50\text{ pF}$, Input $t_r, t_f=20\text{ ns}$, $R_L=200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS All Packages			UNITS	
		MIN.	TYP.	MAX.		
Propagation Delay Time	t_{PHL}	5	—	600	1200	
		10	—	200	400	
		15	—	150	300	
	t_{PLH}	5	—	500	1000	
		10	—	200	400	
		15	—	150	300	
Transition Time	t_{THL}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
	t_{TLH}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
Latch Disable Pulse Width	t_{WH}	5	250	125	—	
		10	100	50	—	
		15	80	40	—	
Address Setup Time	t_{SU}	5	60	15	—	
		10	20	-5	—	
		15	10	-5	—	
Address Hold Time	t_H	5	25	-5	—	
		10	20	10	—	
		15	20	10	—	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	pF

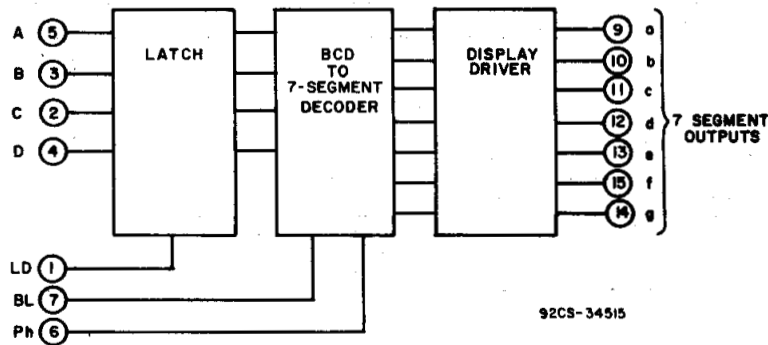


Fig. 4 - BCD-to-seven-segment latch/decoder/driver functional diagram.

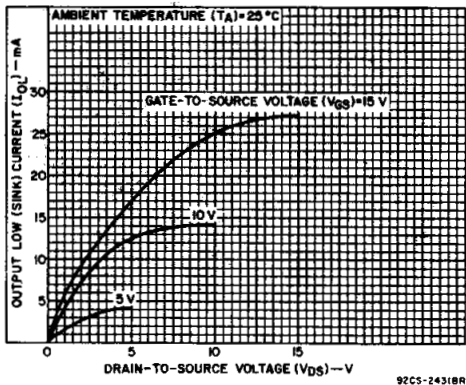


Fig. 5 - Typical output low (sink) current characteristics.

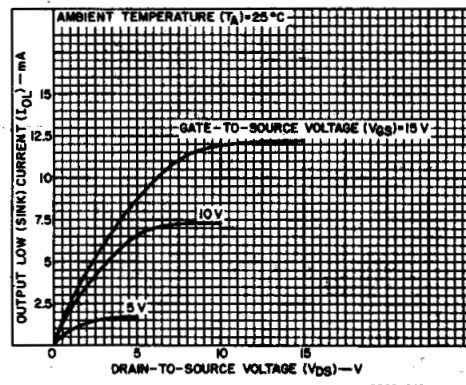


Fig. 6 - Minimum output low (sink) current characteristics.

CD4543B Types

TRUTH TABLE FOR CD4543B

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	
X	1	0	X	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1	1	0	1	1	0	1	1
1	0	0	0	0	1	1	1	1	1	1	0	0	1	1
1	0	0	0	1	0	0	0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0	1	1	0	1	1	1
1	0	0	0	1	1	1	1	1	1	0	0	0	0	0
1	0	0	1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1	1
1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X=Don't care.
 †=Above combinations.
 *=For liquid-crystal readouts, apply a square wave to Ph.
 For common cathode LED readouts, select Ph=0.
 For common anode LED readouts, select Ph=1.
 **=Depends upon the BCD code previously applied when LD=1.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

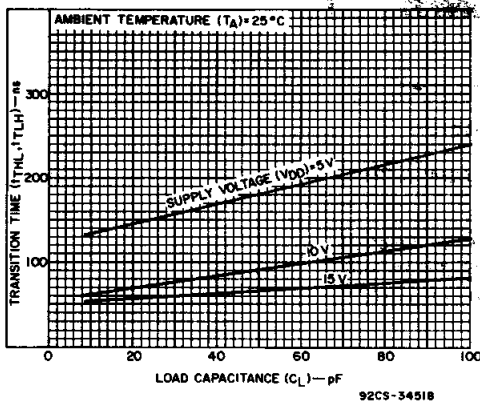


Fig. 7 - Typical transition time as a function of load capacitance.

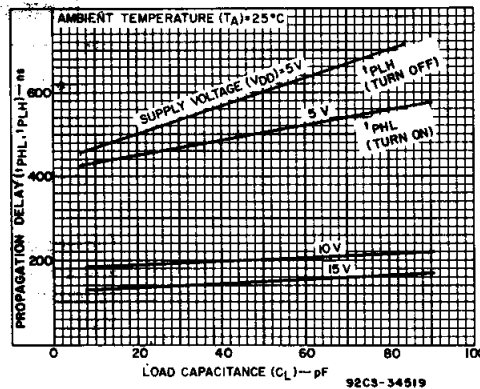


Fig. 8 - Typical propagation delay time as a function of load capacitance.

CD4543B Types

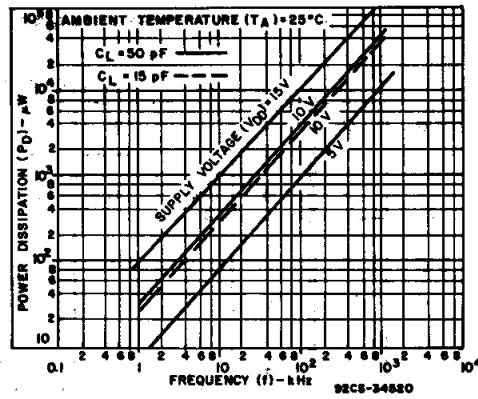


Fig. 9 - Typical dynamic power dissipation as a function of frequency.

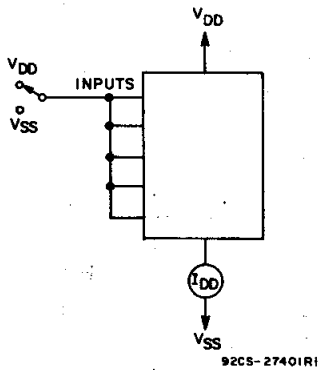


Fig. 10 - Quiescent device current test circuit.

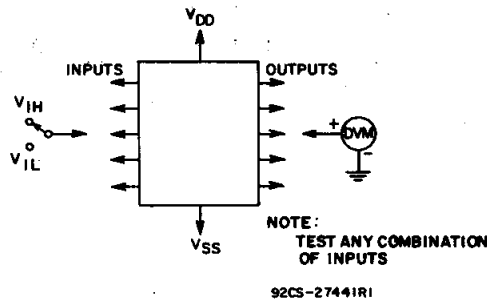


Fig. 11 - Input voltage test circuit.

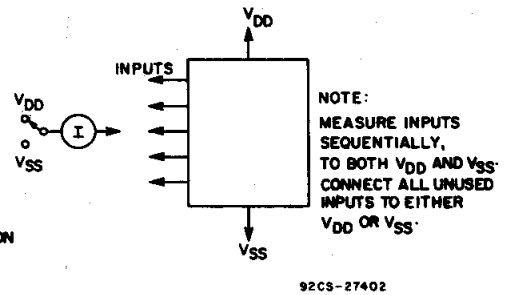
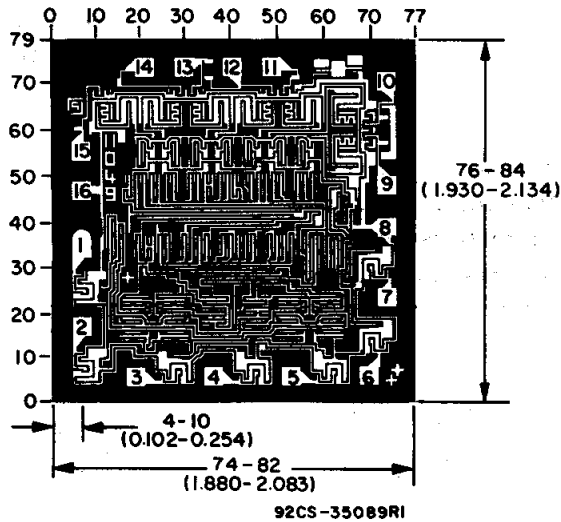


Fig. 12 - Input current test circuit.



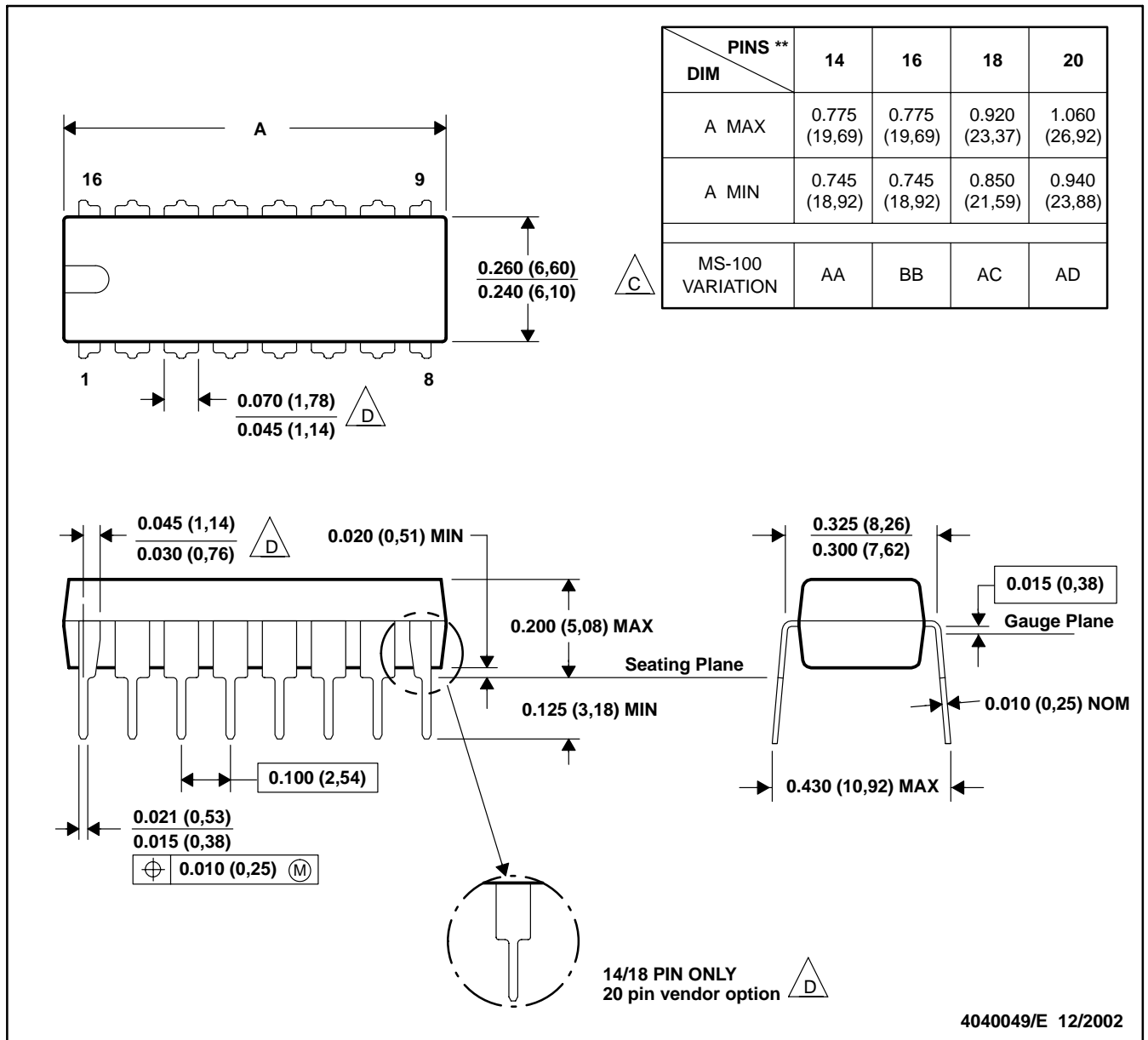
Dimensions and pad layout for CD4543BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

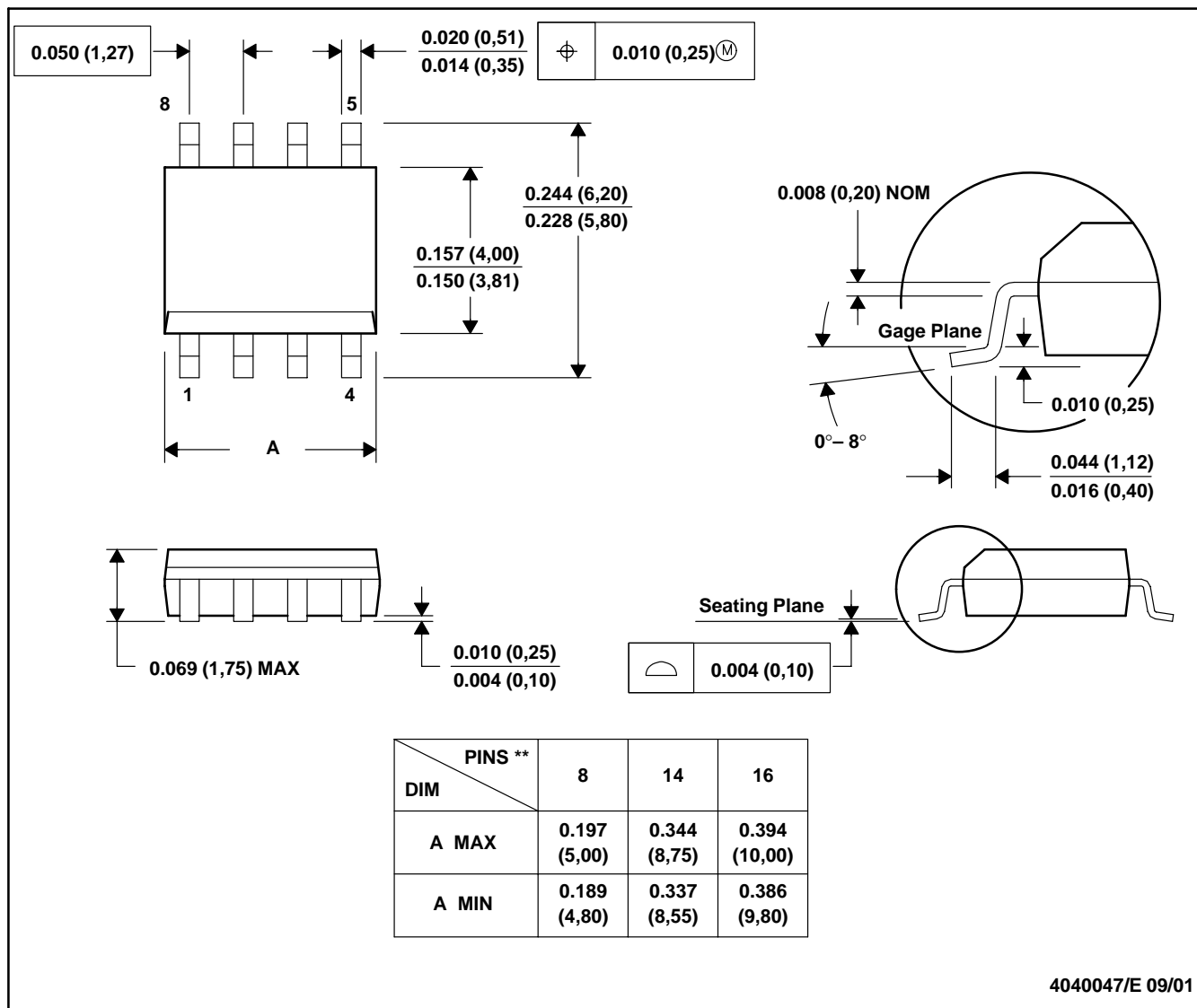


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

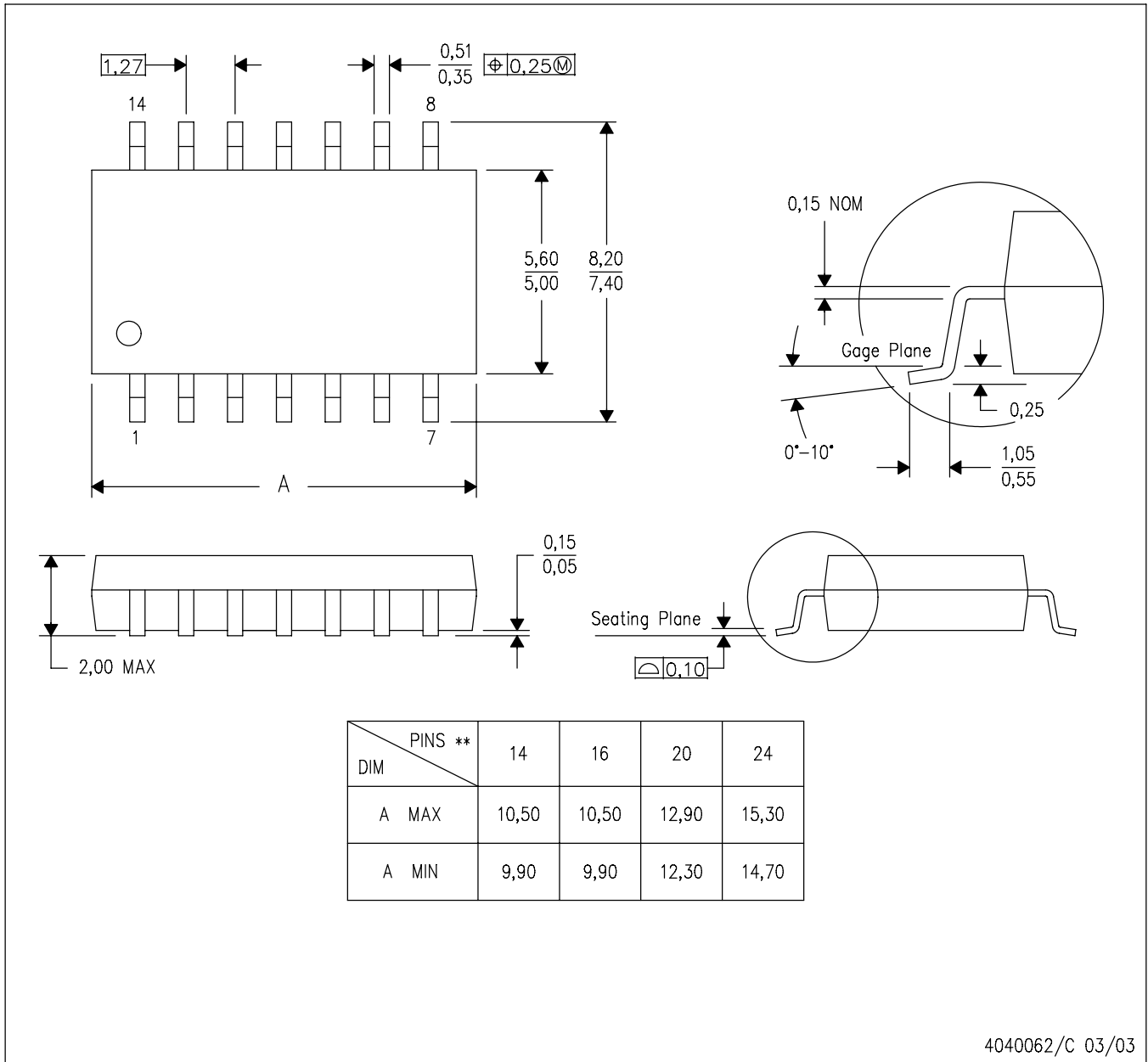


4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

NS (R-PDSO-G**)
14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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[APPLICATION NOTES](#) | [USER GUIDES](#) | [MORE LITERATURE](#)

PRODUCT SUPPORT: [TRAINING](#)

CD4543B, CMOS BCD-to-Seven-Segment Latch/Decoder/Driver for Liquid-Crystal Displays

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4543B
Voltage Nodes (V)	5, 10, 15

FEATURES

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- Display blanking of all illegal input combinations
- Latch storage of code
- Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range
- Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})
- Direct LED driving capability
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Applications:
 - Instrument display driver
 - Dashboard display driver
 - Computer/calculator display driver
 - Timing device driver (clocks, watches, timers)

DESCRIPTION

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CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS} . It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

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TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: [cd4543b.pdf](#) (362 KB, Rev.B) (Updated: 03/12/2003)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits \(SZZA026](#) - Updated: 06/20/2001)
- [Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics \(SCHA004](#) - Updated: 12/03/2001)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\) \(SZZA036A](#) - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
CD4543BE	PDIP (N)	16	-55 TO 125	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION Updated Daily							TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
CD4543BE	ACTIVE	PDIP (N) 16	-55 TO 125	View Contents	1KU 0.20	25	>10k*	>10k 28 Apr	4 WKS	Avnet Americas	>1k	BUY NOW
										Newark Electronics Americas	418	BUY NOW
										EBV Electronik Europe	17	BUY NOW
CD4543BM	ACTIVE	SOIC (D) 16	-55 TO 125	View Contents	1KU 0.20	40	0*	>10k 13 May	4 WKS	None Reported View Distributors		
CD4543BM96	ACTIVE	SOIC (D) 16	-55 TO 125	View Contents	1KU 0.20	2500	0*	>10k 13 May	4 WKS	None Reported View Distributors		
CD4543BNSR	ACTIVE	SOP (NS) 16	-55 TO 125	View Contents	1KU 0.48	2000	0*	>10k 08 May	4 WKS	None Reported View Distributors		
CD4543BPW	ACTIVE	TSSOP (PW) 16	-55 TO 125	View Contents	1KU 0.29	90	0*	3150 16 Apr	4 WKS	None Reported View Distributors		
								>10k 08 May		None Reported View Distributors		
CD4543BPWR	ACTIVE	TSSOP (PW) 16	-55 TO 125	View Contents	1KU 0.13	2000	0*	>10k 08 May	4 WKS	None Reported View Distributors		

Table Data Updated on: 4/17/2003