FAIRCHILD SEMICONDUCTOR

January 1998

74VHC74 • 74VHCT74
Dual D-Type Flip Flop with Preset and Clear

General Description

The VHC/VHCT74 is an advanced high speed CMOS Dual D-Flip Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed:
  VHC f_{max} = 170 MHz (typ) at T_A = 25°C
  VHCT f_{max} = 160 MHz (typ) at T_A = 25°C
- High noise immunity:
  VHC $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
  VHCT V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection:
  VHC inputs only
  VHCT inputs and outputs
- Low power dissipation:
  I_{CC} = 2 μA (max) at T_A = 25°C
- **NOTE: ADD EXTERNAL PULL UP RESISTOR TO VHCT OUTPUTS TO DRIVE CMOS INPUTS**

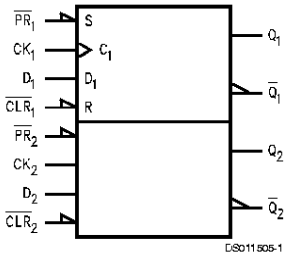
Ordering Code:

Commercial	Package Number	Package Description
74VHC74M	M14A	14-Lead Molded JEDEC SOIC
74VHC74SJ	M14CD	14-Lead Molded EIAJ SOIC
74VHC74MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC74N	N14A	14-Lead Molded DIP
74VHCT74M	M14A	14-Lead Molded JEDEC SOIC
74VHCT74SJ	M14D	14-Lead Molded EIAJ SOIC
74VHCT74MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHCT74N	N14A	14-Lead Molded DIP

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

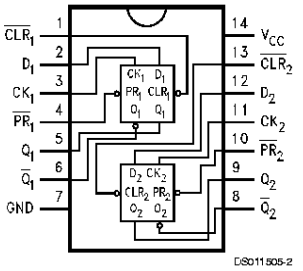
IEEE/IEC



DS011505-1

Connection Diagram

Pin Assignment for DIP, TSSOP and SOIC



DS011505-2

Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Output

Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H*	H*	
H	H	L	↗	L	H	
H	H	H	↗	H	L	
H	H	X	↘	Q_n	Q_n	No Change

* This configuration is nonstable that is it will not persist when preset and clear inputs return to their inactive (high) state

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT (Note 2)	−0.5V to 7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
VHC	±20 mA
VHCT	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	
VHC	2.0V to 5.5V
VHCT	4.5V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
74VHC/VHCT	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC only)	0 ∼ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ∼ 20 ns/V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: V_{OUT} > V_{CC} only if output is in H state.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Characteristics for VHC Family Devices

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	µA	V_{IN} = V_{CC} or GND	

DC Characteristics for VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0				
V_{IL}	Low Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8			
V_{OH}	High Level Output Voltage	4.5	3.15	3.65		3.15		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu A$
		4.5	2.5			2.4				$I_{OH} = -8$ mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\ \mu A$
		4.5			0.36		0.44			$I_{OL} = 8$ mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	µA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	µA	$V_{IN} = V_{CC}$ or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	$V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND	
I_{OFF}	Output Leakage Current (Power Down State)	0.0			+0.5		+5.0	µA	$V_{OUT} = 5.5V$	

AC Electrical Characteristics for VHC

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 ± 0.3	80	125		70		MHz	$C_L = 15$ pF
			50	75		45			$C_L = 50$ pF
		5.0 ± 0.5	130	170		110		MHz	$C_L = 15$ pF
			90	115		75			$C_L = 50$ pF
t_{PLH}, t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	3.3 ± 0.3		6.7	11.9	1.0	14.0	ns	$C_L = 15$ pF
				9.2	15.4	1.0	17.5		$C_L = 50$ pF
		5.0 ± 0.5		4.6	7.3	1.0	8.5	ns	$C_L = 15$ pF
				6.1	9.3	1.0	10.5		$C_L = 50$ pF
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	3.3 ± 0.3		7.6	12.3	1.0	14.5	ns	$C_L = 15$ pF
				10.1	15.8	1.0	18.0		$C_L = 50$ pF
		5.0 ± 0.5		4.8	7.7	1.0	9.0	ns	$C_L = 15$ pF
				6.3	9.7	1.0	11.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			25				pF	(Note 4)

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + $I_{CC}/2$ (per F/F)

AC Operating Requirements for VHC

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = 25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units
			Typ	Guaranteed Minimum		
$t_{W(L)}$	Minimum Pulse Width (CK)	3.3		6.0	7.0	ns
$t_{W(H)}$		5.0		5.0	5.0	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_H	Minimum Hold Time	3.3		0.5	0.5	ns
		5.0		0.5	0.5	
t_{rem}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	3.3		5.0	5.0	ns
		5.0		3.0	3.0	

Note 5: V_{CC} is 3.3 ±0.3V or 5.0 ±0.5V

AC Electrical Characteristics for VHCT

Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock	5.0	100	160		80		MHz	C_L = 15 pF
	Frequency	5.0	80	140		65			C_L = 50 pF
t_{PLH},	Propagation Delay	5.0		5.8	7.8	1.0	9.0	ns	C_L = 15 pF
t_{PHL}	Time (CK-Q, $\overline{Q}$)	5.0		6.3	8.8	1.0	10.0		C_L = 50 pF
t_{PLH},	Propagation Delay Time	5.0		7.6	10.4	1.0	12.0	ns	C_L = 15 pF
t_{PHL}	($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)	5.0		8.1	11.4	1.0	13.0		C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			24				pF	(Note 7)

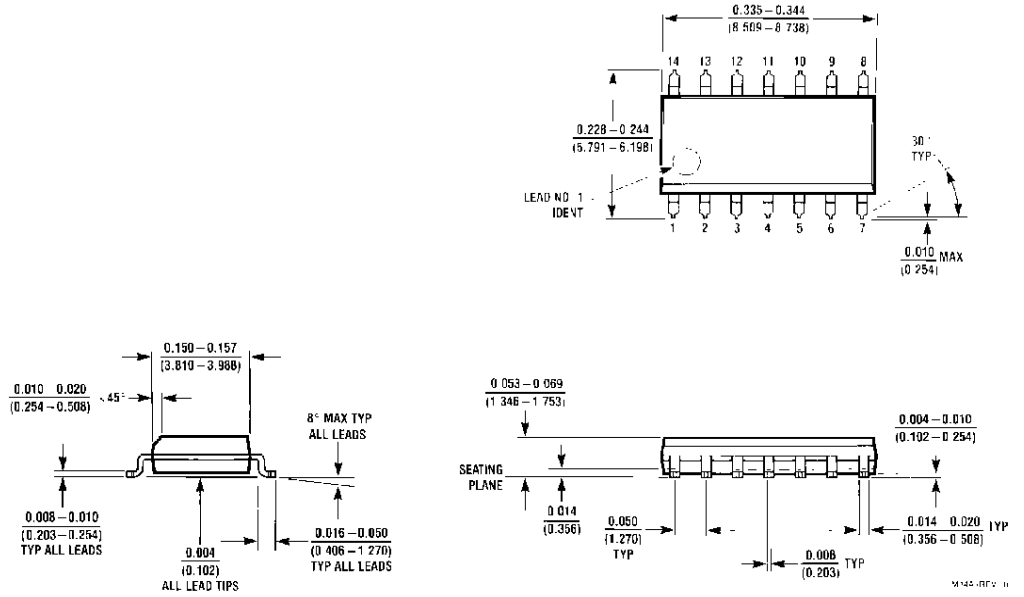
Note 6: V_{CC} is 5.0 ±0.5V

Note 7: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation I_{CC} (opr) = C_{PD} x V_{CC} x f_{IN} + I_{CC}/2 (per flip-flop)

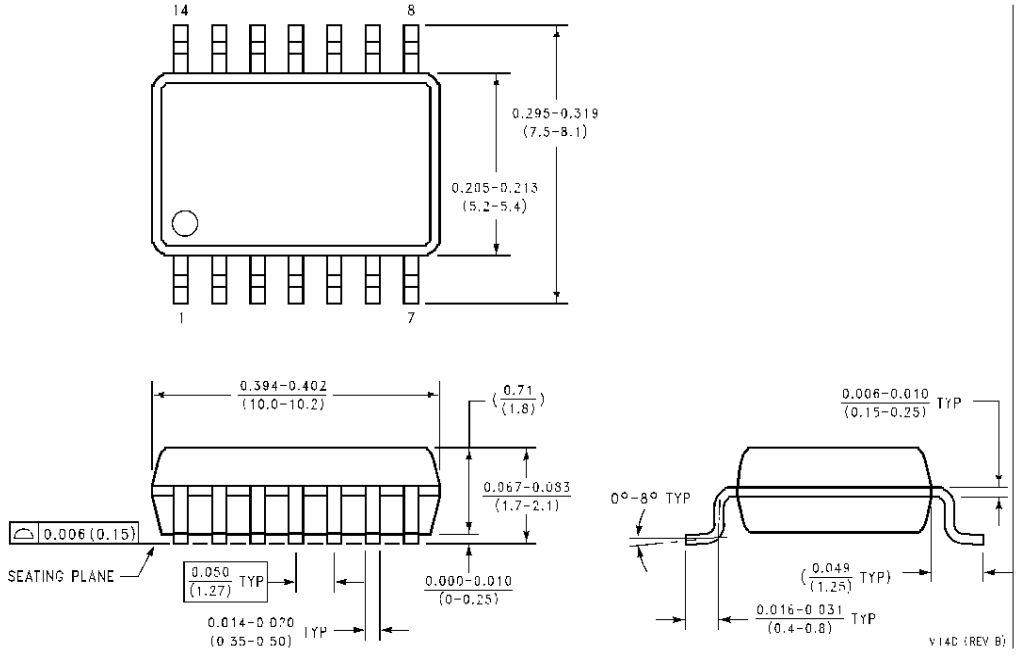
AC Operating Requirements for VHCT

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units
			Typ	Guaranteed Minimum		
$t_{W(L)}$	Minimum Pulse Width (CK)	5.0 ± 0.5			5.0	ns
$t_{W(H)}$						
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		5.0	5.0	ns
t_S	Minimum Setup Time	5.0 ± 0.5		5.0	5.0	ns
t_H	Minimum Hold Time	5.0 ± 0.5		0	0	ns
t_{rem}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		3.5	3.5	ns

Physical Dimensions inches (millimeters) unless otherwise noted

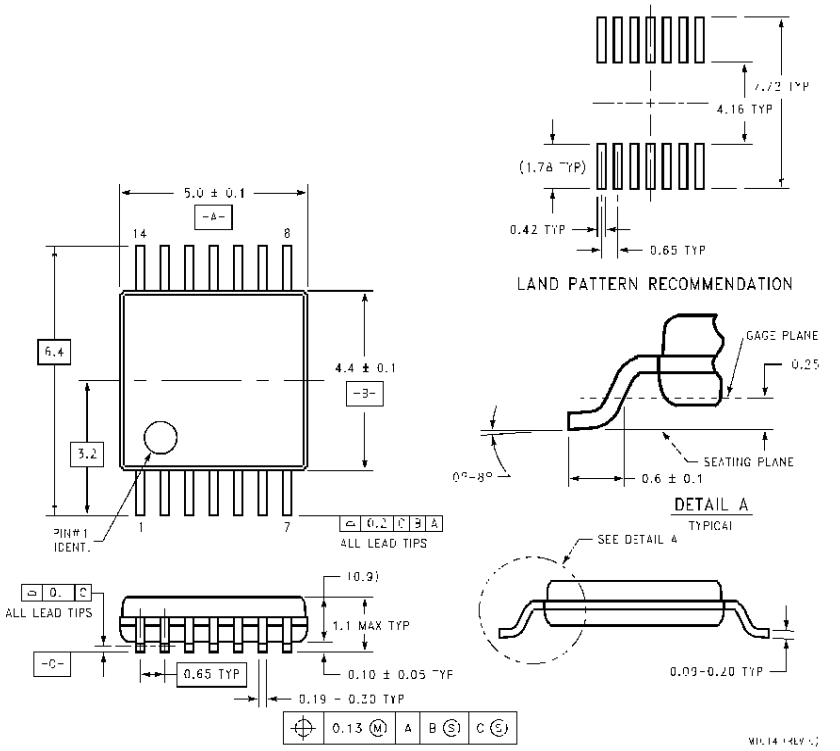


14-Lead Small Outline Integrated Circuit—JEDEC (M)
Package Number M14A



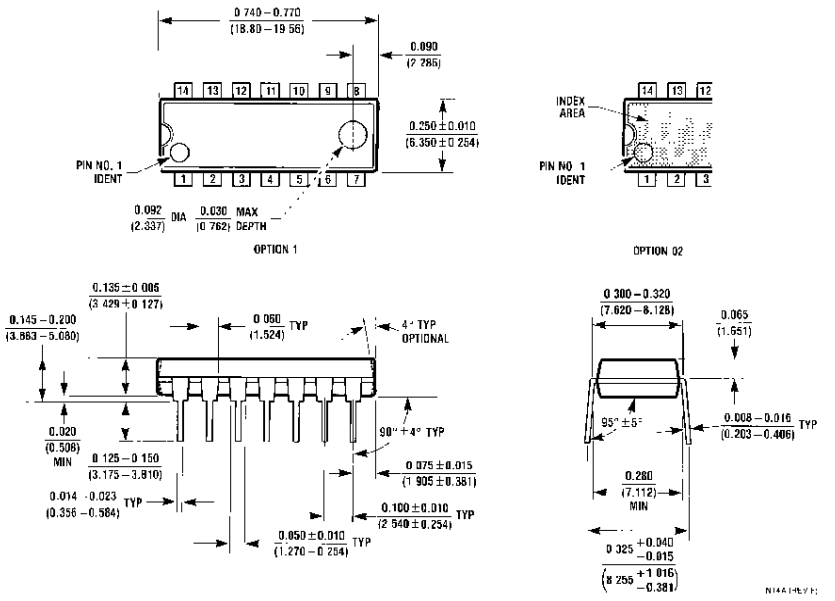
14-Lead Small Outline Package - EIAJ (SJ)
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic JEDEC TSSOP Type 1 (MTC)
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual In-Line Package
Package Number N14A

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