

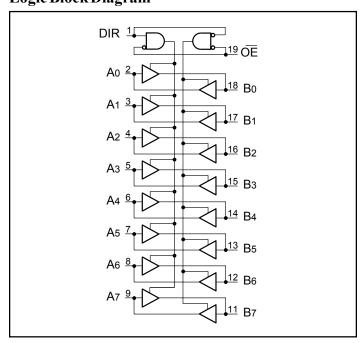


3.3V 8-Bit Bi-Directional Transceiver with 3-State Outputs

Product Features

- Advanced low power CMOS design for 2.7V to 3.6V V_CCoperation
- Supports 5V input/output tolerance in mixed signal mode operation
- Function compatible with LVT family of products
- Balanced ±24mA output drive
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC}=3.3V, $T_A=25$ °C
- I_{off} and Power Up/Down 3-State support live insertion
- Bus Hold on data inputs eliminates the need for external pull-up/down resistors
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
 - -2000V Human-Body Model (A114-B)
 - 200V Machine Model (A115-A)
- Packages (Pb-Free Available):
 - -20-pin 209-mil wide plastic SSOP (H20)
 - -20-pin 173-mil wide plastic TSSOP (L20)
 - -20-pin 300-mil wide plastic SOIC (S20)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74LVCT series of logic circuits are produced using the Company's advanced CMOS technology, achieving industry leading speed.

The PI74LVCTH245 is a non-inverting 8-bit Bidirectional Transceiver designed for low-voltage 2.7V to 3.6V V_{CC} operation, with the capability of interfacing to the 5V system environment. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable (OE) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The PI74LVCTH245 has "Bus Hold" which retains the data input's last valid logic state whenever the datainput goes to highimpedance, preventing "floating" inputs and eliminating the need for pull-up/down resistors.

When V_{CC} is between 0 to 1.5V during power up or power down, the outputs of the device are in the high-impedance state. To ensure the high-impedance state above 1.5V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The device fully supports live-insertion with its I_{off} and power-up/ down 3-state. The I_{off} circuitry disables the outputs when the power is off, preventing the backflow of damaging current through the device. Power-up/down 3-state places the outputs in the highimpedance state during power up or power down, preventing driver conflict.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V _{CC} –0.5V to +6.5V
Input voltage range, $V_I^{(1)}$ $-0.5V$ to $+6.5V$
Voltage range applied to any output in the
high-impedance or power-off state, $V_0^{(1)}$ 0.5V to +6.5V
Voltage range applied to any output in the
active state, $V_O^{(1),(2)}$ 0.5V to V_{CC} +0.5V
Input clamp current, I _{IK} (V _I <0)–50mA
Output clamp current, I _{OK} (V _O <0) –50mA
Continous Output Current I _O ±50mA
Continous Current through each V _{CC} or GND pin ±100mA
Package thermal impedance, θ _{JA} (3): package H 81°C/W
package L 84°C/W
package S 84°C/W
Storage Temperature range, T _{stg} –65°C to 150°C

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

- 1. Input negative-voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This value is limited to 6.5V maximum.
- $3. \, The \, package \, thermal \, impedance \, is \, calculated \, in \, accordance \, with \, JESD \, 51.$

Truth Table⁽⁴⁾

Inpu	Outputs	
OE	DIR	
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	X	Z

Notes:

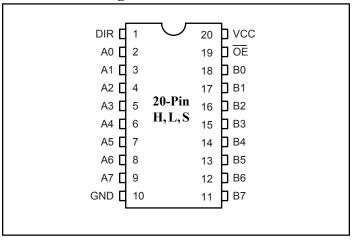
- 4. H = High Signal Level
 - L = Low Signal Level
 - X = Don't Care or Irrelevant
 - Z = High Impedance

Product Pin Description

Pin Name	Description				
ŌĒ	3-State Output Enable Inputs (Active LOW)				
DIR	Direction Control Input				
xAx	Side A Inputs or 3-State Outputs				
xBx	Side B Inputs or 3-State Outputs				
GND	Ground				
V_{CC}	Power				

Product Pin Configuration

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Recommended Operating Conditions⁽⁵⁾

		Min.	Max.	Units	
V _{CC} Supply Voltage	Operating	2.7	3.6		
V _{IH} High-level Input Voltage	$V_{CC} = 2.7V \text{ to } 3.6V$	2.0			
V _{IL} Low-level Input Voltage	$V_{CC} = 2.7V \text{ to } 3.6V$		0.8		
V _I Input Voltage		0	5.5	V	
V Outrot Valence	High or Low State	0	V _{CC}		
V _O Output Voltage	3-State	0	5.5		
I _{OH} High-level output current	$V_{CC} = 2.7V$		- 12	mA	
	$V_{CC} = 3.0 \text{V to } 3.6 \text{V}$		- 24		
	$V_{CC} = 2.7V$		12		
I _{OL} Low-level output current	$V_{CC} = 3.0 \text{V to } 3.6 \text{V}$		24		
$\Delta t/\Delta V$ Input transition rise or fall rate			6	ns/V	
Δt/ΔV _{CC} Power-up ramp rate		150		μs/V	
T _A Operating free-air temperature	•	- 40	85	°C	

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Notes: 5. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

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DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters	Description	1	Tes	t Conditions		Min.	Max.	Units	
V _{IK}	Clamp Diode Voltage		$V_{CC} = 2.7V$	$I_I = -18\text{mA}$			-1.2V		
		$V_{CC} = 2.7V \text{ to} $ 3.6V	I _{OH} = -100μA		V _{CC} -0.2V				
1 .7	Output High Voltage		$V_{\rm CC} = 2.7V$ $I_{\rm OH} = -12 \mathrm{mA}$		2.2				
V_{OH}			$V_{CC} = 3V$	$I_{OH} = -12 \text{mA}$		2.4	2.4		
			VW-3V	$I_{OH} = -24 \text{mA}$		2.2		V	
			$V_{CC} = 2.7V \text{ to} $ 3.6V	I _{OL} = 100μA			0.2	-	
V_{OL}	Output Low Voltage		$V_{CC} = 2.7V$	I _{OL} = 12mA			0.4		
			$V_{CC} = 3V$	I _{OL} = 12mA			0.4		
				I _{OL} = 24mA			0.55	†	
		Control Inputs	$V_{CC} = 0V$ to 3.6V	$V_I = 0V$ to 5.5V			±5		
I_{I}	Input Leakage Current	A or B Ports ⁽⁶⁾	$V_{CC} = 3.6V$	$V_{I} = 5.5V$					
-1				V _I =V _{CC}			±5		
				V _I =GND					
	Data Input Hold Current (A or B ports)	•	V 2V	$V_I = 0.8V$		75			
I _{I(HOLD)}		ent	$V_{CC} = 3V$	$V_I = 2V$		-75			
			$V_{CC} = 3.6V^{(7)}$	$V_{\rm I} = 0 \text{ to } 3.6 \text{V}$			±500		
$I_{O\!F\!F}$	Power Off Output Leakage Current		$V_{CC} = 0V$	$V_{\rm I}$ or $V_{\rm O}$ = 0V to	5.5V		±5		
$I_{O\!Z\!PU}$	Power-Up 3-State Current		$V_{CC} = 0V$ to 1.5V	$V_O = 0.5V$ to 5.5V $\overline{OE} = \text{don't care}$	V,		±5	μА	
I _{OZPD}	Power-Down 3-State Current		$V_{\rm CC}$ = 1.5V to 0V	$V_O = 0.5V$ to 5.57 $\overline{OE} = \text{don't care}$	V,		±5		
I _{CC} Quiescent Power Supply Current	Quiescent Power Supply	Ouiescent Power Supply $V_{CC} = 2.7V$ to	$V_{CC} = 2.7V$ to	V _I = V _{CC} or GND			100		
		3.6V	$3.6V \le V_I \le 5.5V^{(8)}$	$I_O = 0$		100			
ΔI_{CC}	Increase in $I_{\mathbb{C}}$		$V_{CC} = 3.0 \text{V to} $ 3.6 V	One input at V_{CC} - Other inputs at V_{CC} GND			500		

Notes: 6. For I/O ports, Input Leakage Current (I_I) includes the 3-state Output Leakage Current. Unused pins are at V_{CC} or GND.

- 8. This applies in the diabled stae only.
- 9. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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^{7.} This is the maximum bus-hold dynamic current. It is the minimum overdrive current required to switch the input from one state to another.



Capacitance

Parameters	Description	Test Conditions	Typ. ⁽¹⁰⁾	Units
C_{IN}	Control Input Capacitance	V_{CC} = 3.3V, V_{I} = V_{CC} or GND	3.3	
C_{IO}	Input/Output Capacitance	V_{CC} = 3.3V, V_{O} = V_{CC} or GND	7.8	pF
C_{PD}	Power Dissipation Capacitance (11)	V_{CC} = 3.3V, V_{I} = 0V or V_{CC} , f=10 MHz	33	

Notes:

10. All typical values are measured at $V_{CC} = 3.3V$, $T_A = 25$ °C.

11. C_{PD} is defined as the value of the internal equivalent capacitance withic is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle, C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN})+(I_{CC}\text{static})$.

Switching Characteristics Over Operating Range

		Eurona	Tr.	$V_{CC} = 3.3V \pm 0.3V$		$V_{\rm CC} = 2.7 V$							
Parameters	Description	From (Input)	-	$C_{L} = 50 pF, R_{L} = 500 Ohm$		$C_L = 50 pF, R_L = 500 Ohm$		Units					
				Min.	Max.	Min.	Max.						
t _{PLH}	Propagation	A or B	B or A	1.0	5.4	1.0	5.8						
tPHL	Delay		D OI A	1.0	5.4	1.0	5.8						
tPZH	Output Enable	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌE	Output Enable	A am D	1.0	7.0	1.0	7.9	
t _{PZL}	Time						A or B	1.0	7.0	1.0	7.9	ns	
t _{PHZ}	Output Disable Time $\overline{\mathrm{OE}}$	ŌĒ	ŌĒ	— OF	e -	A D	1.0	5.4	1.0	5.8			
tPLZ				A or B	1.0	5.4	1.0	5.8					
t _{SK(O)}	Output to Output Skew ⁽¹²⁾				0.5								

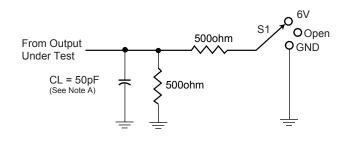
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Notes:

12. Skew between any two outputs, switching in the same direction.



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7V$ and $3.3V \pm 0.3V$

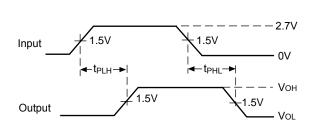


Load Circuit

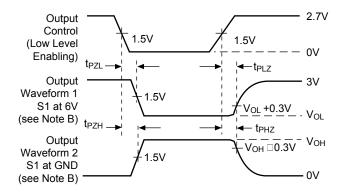
Test	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	6V
t _{PHZ} /t _{PZH}	GND

1.5V 1.5V 2.7V

Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50$ ohm, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.

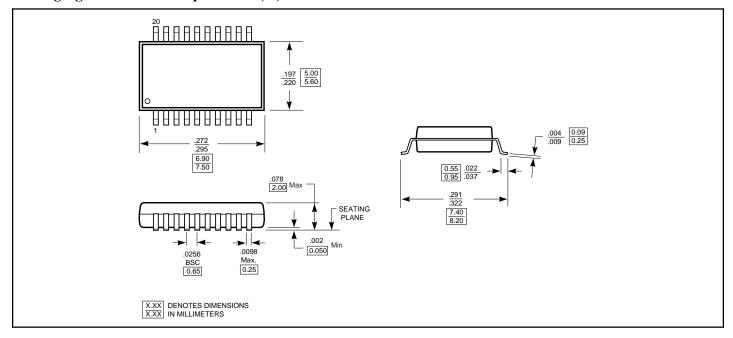
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D. The outputs are measured one at a time with one transition per measurement.

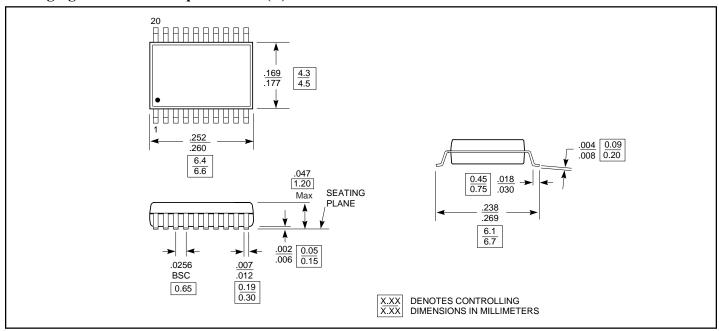
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Packaging Mechanical: 20-pin SSOP (H)

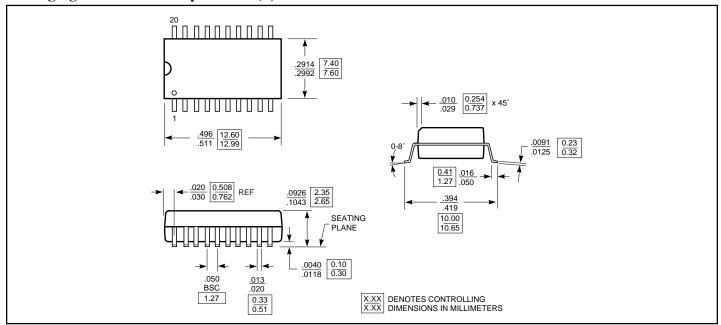


Packaging Mechanical: 20-pin TSSOP (L)





Packaging Mechanical: 20-pin SOIC (S)



Ordering Information

Ordering Data	Description
PI74LVCTH245H	20-pin, 209-mil wide plastic SSOP
PI74LVCTH245L	20-pin, 173-mil wide plastic TSSOP
PI74LVTCH245S	20-pin, 300-mil wide plastic SOIC

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/mechanicals.php

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