High Speed CMOS 8-Bit Register with Asynchronous Reset

QS54/74FCT273T

QS54/74FCT2273T

FEATURES/BENEFITS

- Pin and function compatible to the 74F273 74FCT273 and 74ABT273
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 273T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A , C & D speed grades with 4.4 ns t_{PD} for D
- I_{OL} = 48 mA Com., 32 mA Mil.

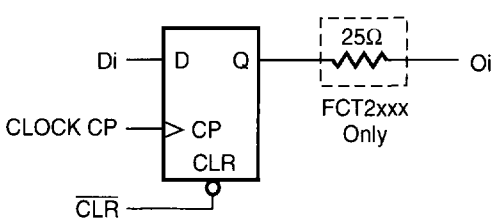
FCT-T 2273T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. thru D speed grades with 5.0 ns t_{PD} for D
- I_{OL} = 12 mA Com.

DESCRIPTION

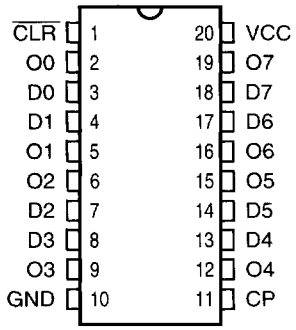
The QSFCT273T and QSFCT2273T are high-speed CMOS TTL-compatible registers with an asynchronous reset input. They are 8-bit registers with a buffered common clock and a buffered output drive. The QSFCT2273T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock. The high output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

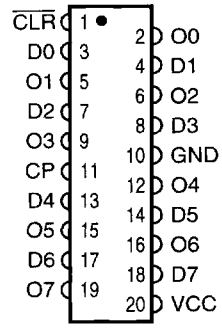


PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



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PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CP	I	Clock Input
$\overline{CLR}$	I	Clear Input

FUNCTION TABLE

Inputs $\overline{CLR}$	Inputs CP	Inputs Di	Internal Q Value	Outputs Oi	Function
L	X	X	L	L	Clear Register
H	↑	L	L	L	Load Input Data
H	↑	H	H	H	Load Input Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1,3,4,7,8,11,12,3,1417,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
—	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Qccd	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., 0 ≤ V_{IN} < Vcc	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX – 25Ω)	Vcc = Min., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min. I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	Vcc = Min. I_{OL} = 32 mA (MIL) I_{OL} = 48 mA (COM)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = −55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		273 2273 Min	273 2273 Max	273A 2273A Min	273A 2273A Max	273C 2273C Min	273C 2273C Max	273D 2273D Min	273D 2273D Max	Unit
t_{PHL}	Propagation Delay	COM	2	13	2	7.2	2	5.2	1.5	4.4	ns
t_{PLH}	CP, $\overline{CLR}$ to Oi (273)	MIL	2	15	2	8.3	—	—	—	—	
t_{PHL}	Propagation Delay	COM	2	13	2	7.2	2	5.2	1.5	5.0	ns
t_{PLH}	CP, $\overline{CLR}$ to Oi (2273)	MIL	2	15	2	8.3	—	—	—	—	
t_S	Data Setup Time	COM	3	—	2	—	1.5	—	1.5	—	ns
	Di to CP	MIL	3.5	—	2	—	—	—	—	—	
t_H	Data Hold Time Time	COM	2	—	1.5	—	1	—	1	—	ns
	Di to CP	MIL	2	—	1.5	—	—	—	—	—	
t_{WCP}	Clock Pulse Width	COM[2]	7	—	6	—	4	—	3	—	ns
	HIGH or LOW	MIL[2]	7	—	6	—	—	—	—	—	
t_{WCLR}	$\overline{CLR}$ Pulse Width	COM[2]	7	—	6	—	5	—	3	—	ns
	HIGH or LOW	MIL[2]	7	—	6	—	—	—	—	—	
t_{REC}	$\overline{CLR}$ Recovery Time	COM[2]	4	—	2	—	1.5	—	1.5	—	ns
	$\overline{CLR}$ to CP	MIL[2]	5	—	2.5	—	—	—	—	—	

Notes:
1. Minimums guaranteed but not tested for all parameters except t_S and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.