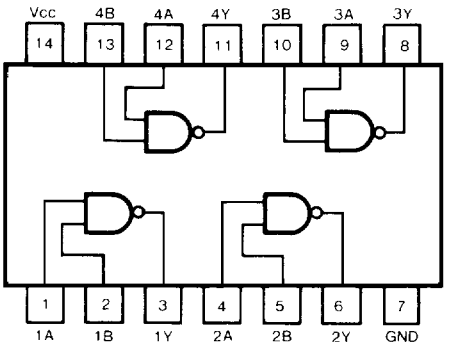
GD54/74LS00

QUADRUPLE 2-INPUT POSITIVE NAND GATES

Description

This device contains four independent 2-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B}$ or $Y=\overline{A}+\overline{B}$ in positive logic.

Pin Configuration

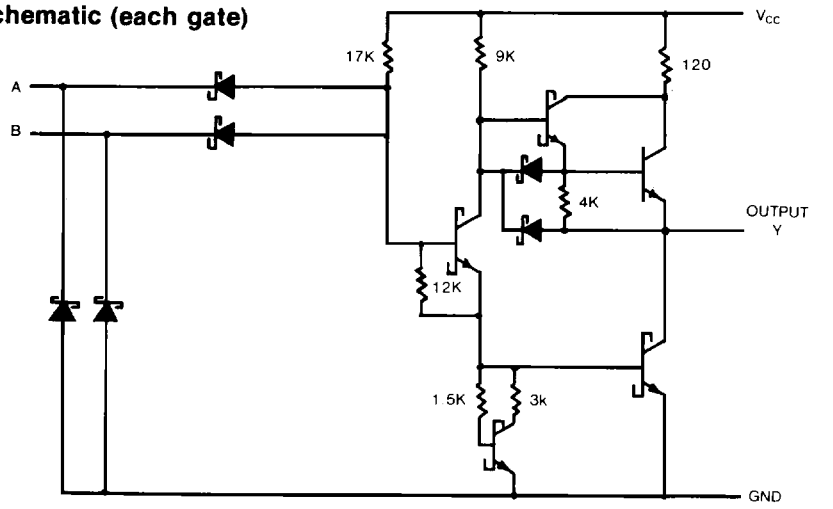


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	μA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.8	1.6	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				2.4	4.4	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

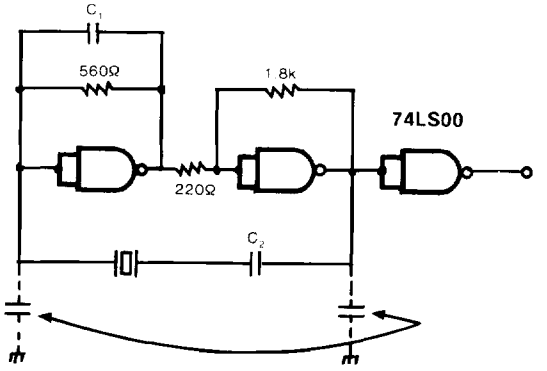
SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

#For load circuit and voltage waveforms, see page 3-11.

Application Example

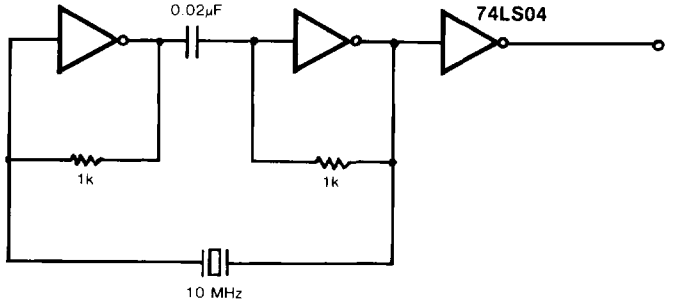
Crystal Clock Generator

(1) GD74LS00



Frequency (MHz)	C_1(pF)	C_2(pF)
1∼ 3	47	24
3∼ 4	47	22
4∼ 6	22	24
6∼ 8	22	22
8∼10	10	20
10∼13	0	20
13∼16	0	18

(2) GD74LS04



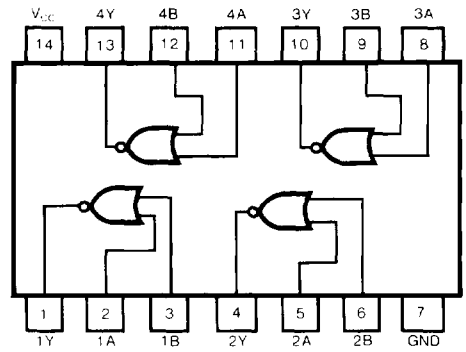
GD54/74LS02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

Description

This device contains four independent 2-input NOR gates. It performs the Boolean functions $Y=\overline{A}\cdot\overline{B}$ or $Y=\overline{A+B}$ in positive logic.

Pin Configuration

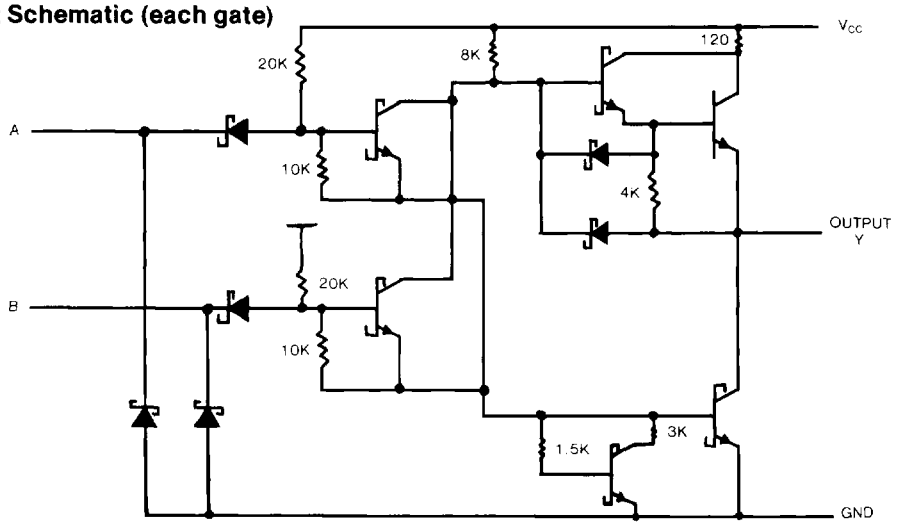


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C