

10-bit bus interface latch (3-State)

74ABT841

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable (\overline{OE}) is Low. When \overline{OE} is High the output is in the High-impedance state.

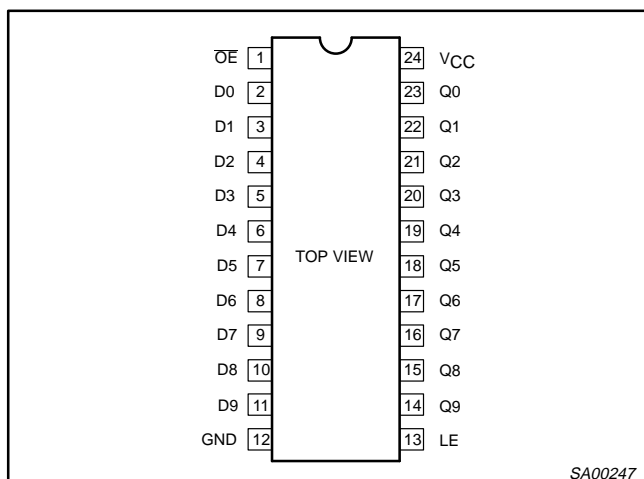
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	4.1	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	−40°C to +85°C	74ABT841 N	74ABT841 N	SOT222-1
24-Pin plastic SO	−40°C to +85°C	74ABT841 D	74ABT841 D	SOT137-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT841 DB	74ABT841 DB	SOT340-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT841 PW	74ABT841PW DH	SOT355-1

PIN CONFIGURATION



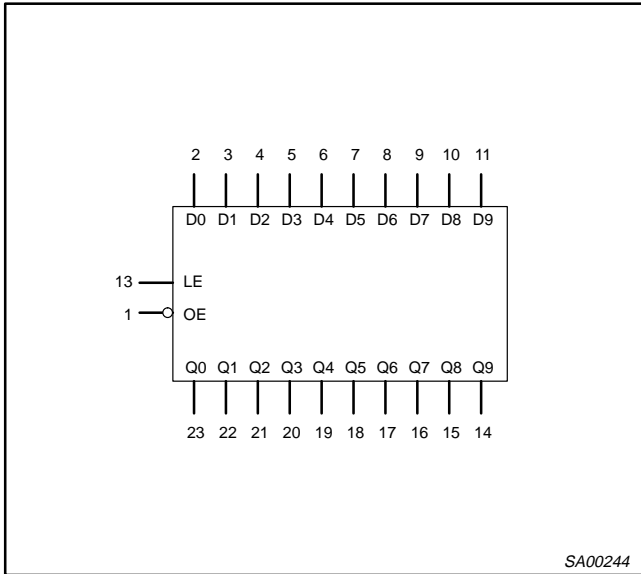
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	\overline{OE}	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0-D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0-Q9	Data outputs
13	LE	Latch enable input (active falling edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

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LOGIC SYMBOL

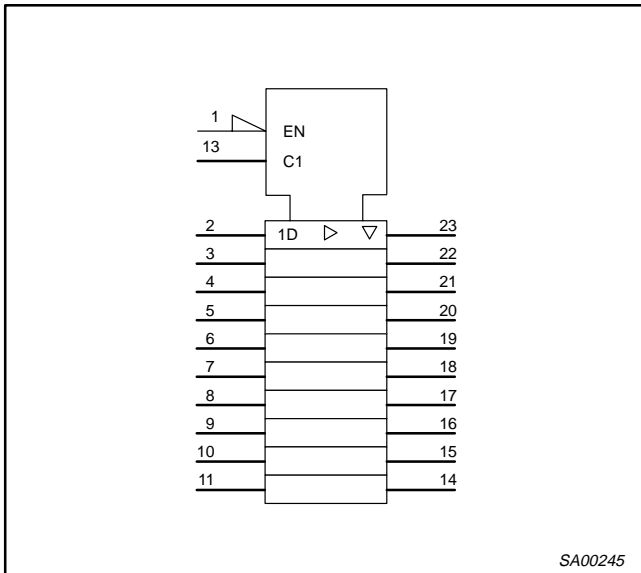


FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
\overline{OE}	LE	Dn	Q0 – Q9	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low LE transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low LE transition
- ↓ = High-to-Low LE transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state

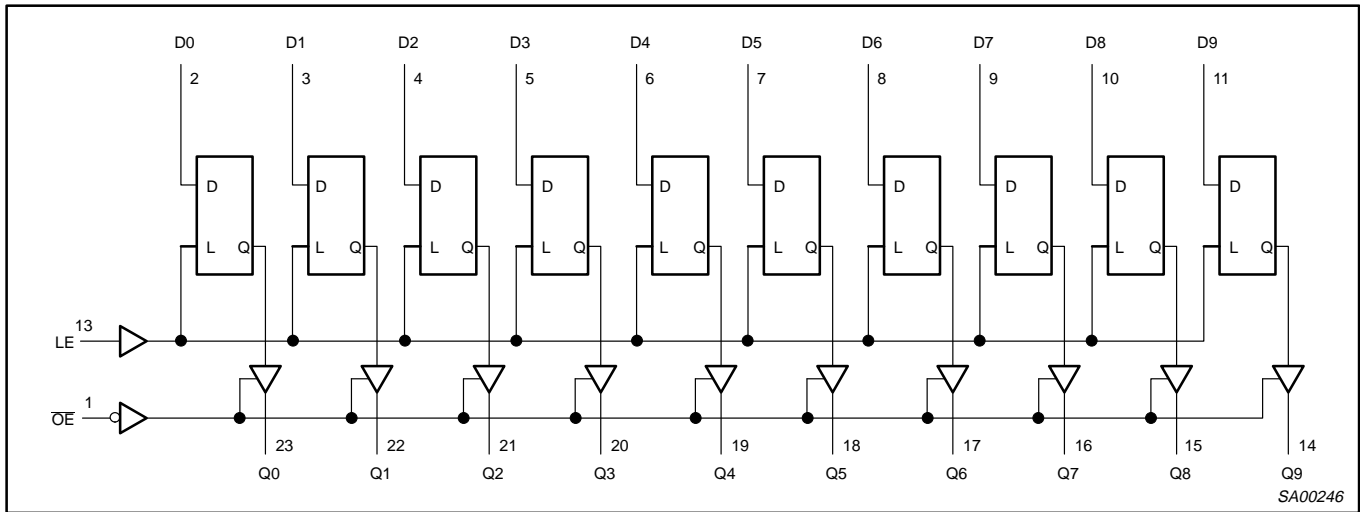
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	3.5		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	4.0		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.6		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins		±0.01	±1.0		±1.0	μA
		Data pins		±5	±100		±100	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-state output current ⁴	V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = V _{CC}		±5.0	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{IL} + I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	μA
I _{CEX}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		25	38		38	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	One input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100μsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	2	2.1 2.0	4.1 4.0	5.5 5.5	2.1 2.0	6.2 6.2	ns
t _{PLH} t _{PHL}	Propagation delay LE to Qn	1	2.1 2.8	4.1 4.6	5.9 6.2	2.1 2.8	6.5 6.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.0 2.2	3.0 4.1	4.5 5.6	1.0 2.2	5.3 6.3	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	2.7 2.8	4.7 4.6	6.2 6.1	2.7 2.8	7.1 6.5	ns

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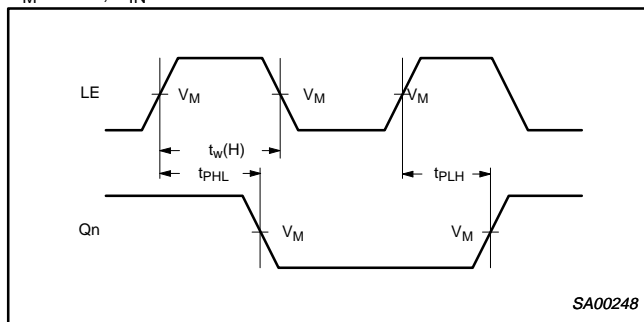
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

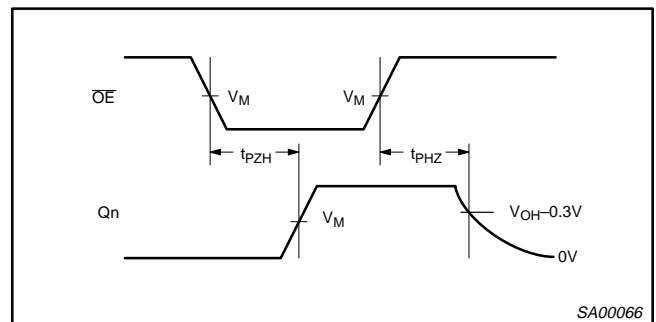
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to LE	3	2.5 1.5	1.0 0.0	2.5 1.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to LE	3	1.5 1.0	0.2 -0.8	1.5 1.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	LE pulse width High or Low	1	3.3	1.9	3.3	ns

AC WAVEFORMS

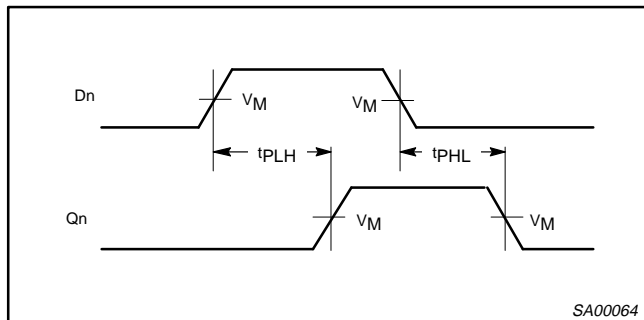
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



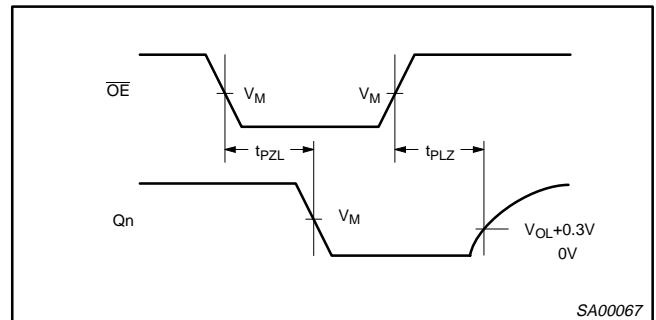
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



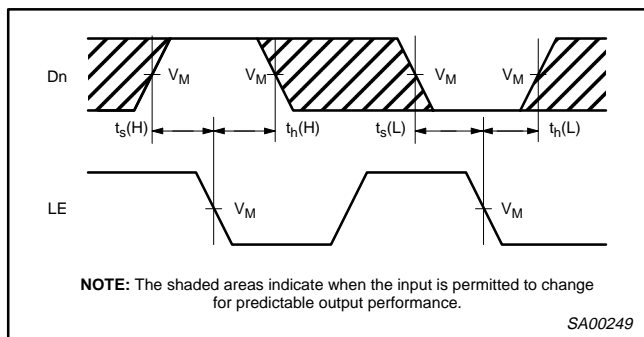
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

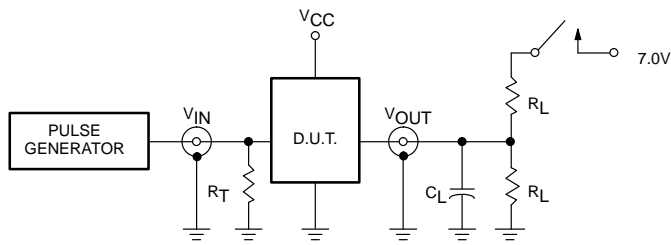


Waveform 3. Data Setup and Hold Times

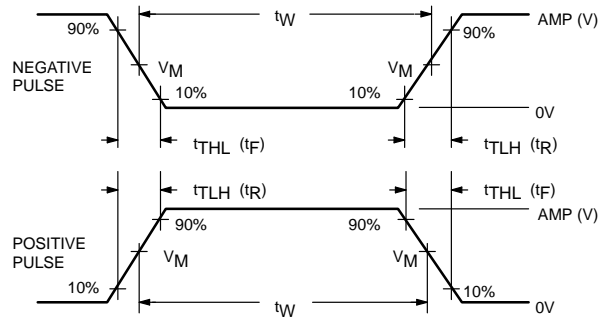
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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _W	t _R	t _F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012