



Integrated Device Technology, Inc.

# 3.3V CMOS SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

## IDT74ALVC1G79 ADVANCE INFORMATION

### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.65mm pitch PSOP package
- Extended commercial range of - 40°C to + 85°C
- V<sub>CC</sub> = 3.3V ± 0.3V, Normal Range
- V<sub>CC</sub> = 1.65V to 3.6V, Extended Range
- V<sub>CC</sub> = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

### Drive Features for ALVC1G79:

- High Output Drivers: ±24mA
- Suitable for heavy loads

### APPLICATIONS:

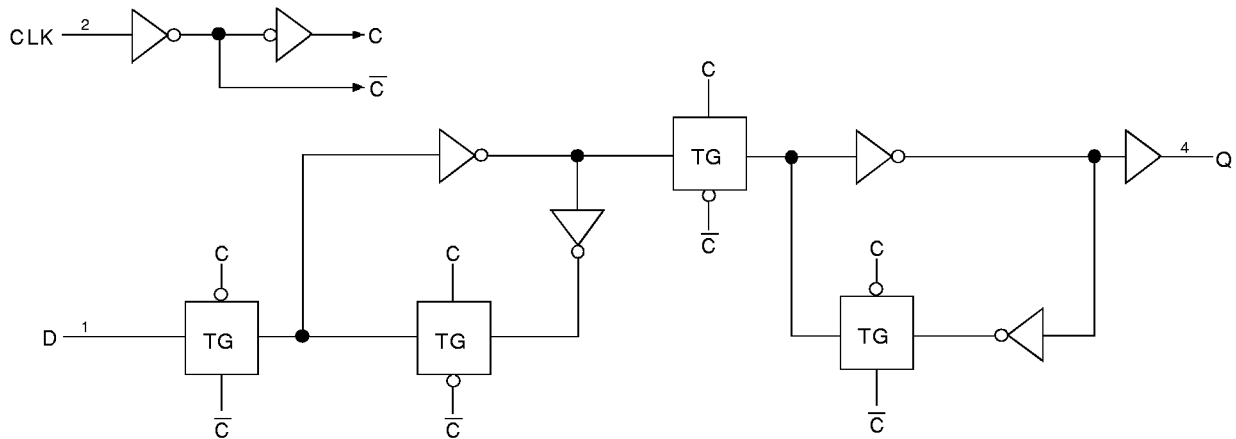
- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

### DESCRIPTION:

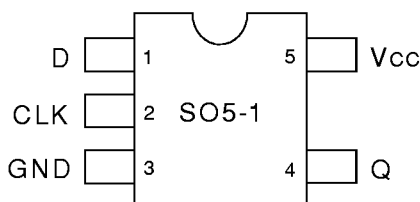
This single positive-edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. The ALVC1G79 is designed for 1.65V to 3.6V V<sub>CC</sub> operation. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The ALVC1G79 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION



PSOP  
TOP VIEW

### PIN DESCRIPTION

Pin Names	Description
CLK	Clock Input
D	Data Input
Q	Data Output

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**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**JANUARY 1999**

**FUNCTION TABLE<sup>(1)</sup>**

Inputs		Output
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q <sub>0</sub>

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH Transition  
Q<sub>0</sub> = Level of Q before the indicated steady-state input conditions were established

**ABSOLUTE MAXIMUM RATING<sup>(1)</sup>**

Symbol	Description	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> + 0.5	V
T <sub>STG</sub>	Storage Temperature	- 65 to + 150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to + 50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	± 50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

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**NOTE:**

- As applicable to the device type.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C, V<sub>CC</sub> = 2.3V to 3.6V

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 1.65V to 1.95V		0.65 x V <sub>CC</sub>	—	—	V
		V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 1.65V to 1.95V		—	—	0.35 x V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	± 5	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	± 5	
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V		—	—	± 10	µA
		V <sub>O</sub> = GND				± 10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = - 18mA		—	- 0.7	- 1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	10	µA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	µA

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**NOTE:**

- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 1.65V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 1.65V	I <sub>OH</sub> = -4mA	1.2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -24mA	2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 1.65V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 1.65V	I <sub>OL</sub> = 4mA	—	0.45	
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

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### NOTE:

- V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 1.8V ± 0.15V	V <sub>CC</sub> = 2.5 ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typ.	Typ.	Typ.	
CPD	Power Dissipation Capacitance	CL = 0pF, f = 10MHz	—	—	—	pF

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		—	—	—	—	—	—	—	—	MHz
t <sub>PLH</sub>	Propagation Delay CLK to Q	—	12	—	6	—	5	—	3.8	ns
t <sub>PHL</sub>										
t <sub>w</sub>	Pulse Width, CLK HIGH or LOW	5	—	3.3	—	3.3	—	3.3	—	ns
t <sub>SU</sub>	Setup Time, data before CLK↑, HIGH	5	—	3	—	3	—	3	—	ns
t <sub>SU</sub>	Setup Time, data before CLK↑, LOW	5	—	3	—	3	—	3	—	ns
t <sub>H</sub>	Hold Time, data after CLK↑	2	—	1	—	1	—	0	—	ns

### NOTE:

- See test circuits and waveforms. T<sub>A</sub> = -40°C to +85°C.

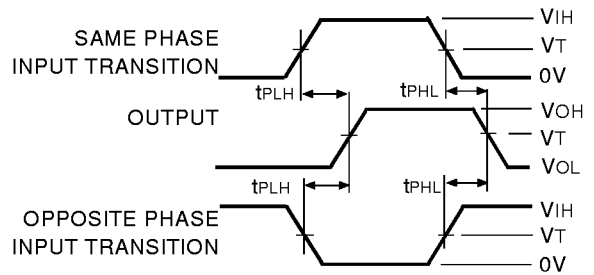
## TEST CIRCUITS AND WAVEFORMS:

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ±0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

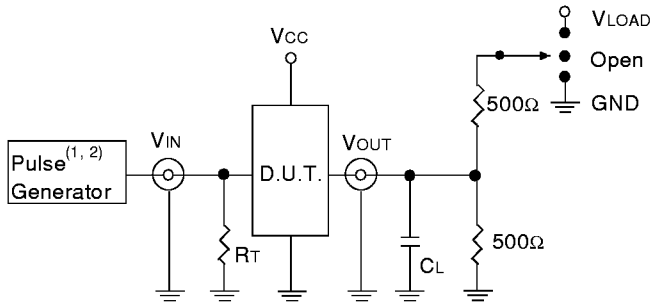
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### PROPAGATION DELAY



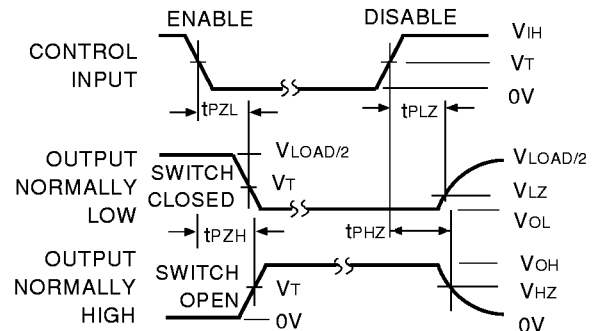
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### TEST CIRCUITS FOR ALL OUTPUTS



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### ENABLE AND DISABLE TIMES



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

#### NOTE:

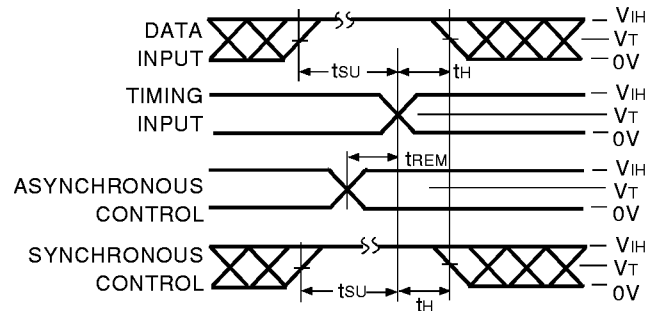
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SWITCH POSITION:

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

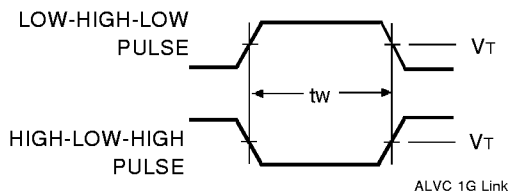
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### SET-UP, HOLD AND RELEASE TIMES



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### PULSE WIDTH



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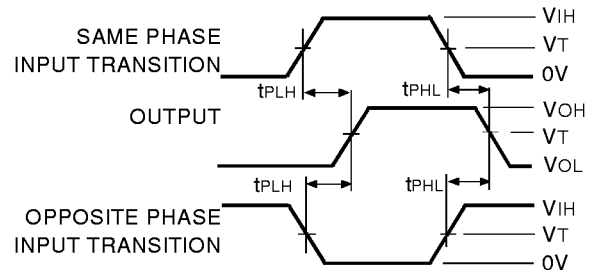
**1.8V ± 0.15V TEST CIRCUITS AND WAVEFORMS:**

**TEST CONDITIONS**

Symbol	V <sub>cc</sub> <sup>(1)</sup> = 1.8V ± 0.15V	Unit
V <sub>LOAD</sub>	2 x V <sub>cc</sub>	V
V <sub>IH</sub>	V <sub>cc</sub>	V
V <sub>T</sub>	V <sub>cc</sub> / 2	V
V <sub>LZ</sub>	150	mV
V <sub>HZ</sub>	150	mV
CL	30	pF

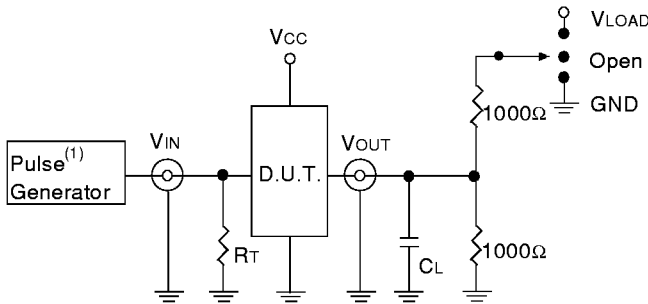
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**PROPAGATION DELAY**



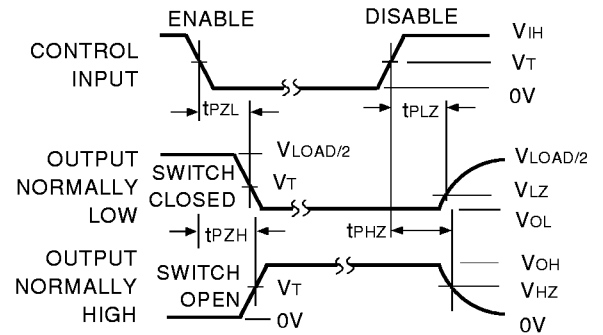
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**TEST CIRCUITS FOR ALL OUTPUTS**



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**SET-UP, HOLD AND RELEASE TIMES**



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**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

**NOTE:**

- 1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>f</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

**NOTE:**

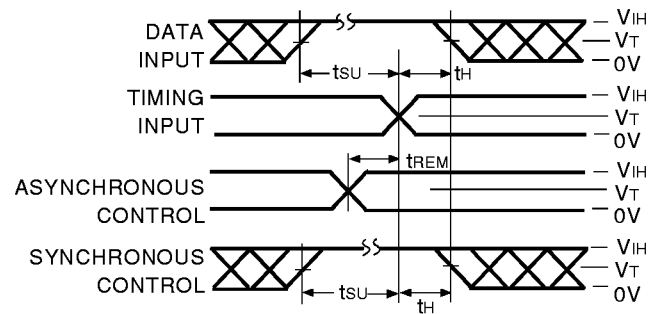
- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

**SWITCH POSITION:**

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

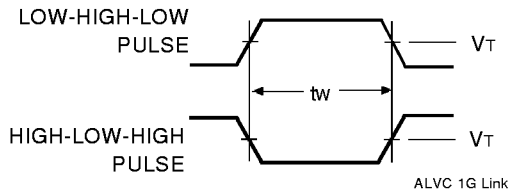
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**ENABLE AND DISABLE TIMES**



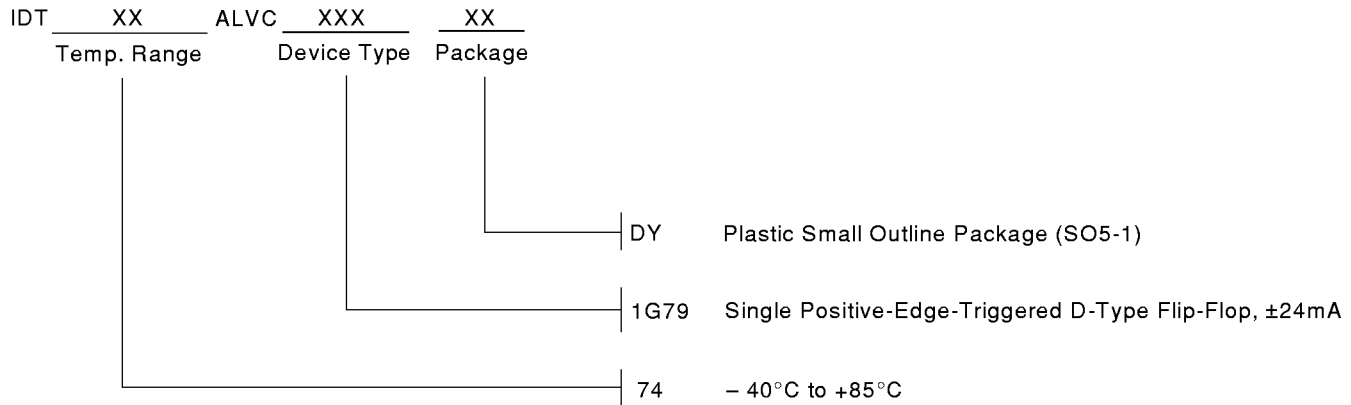
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**PULSE WIDTH**



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## ORDERING INFORMATION



## PICOGATE-LOGIC (DY) PACKAGES

Due to their small size, PicoGate-Logic packages require more complex symbolization guidelines. IDT's 5-pin PSOP (DY) packaged devices utilize a three-symbol name rule. The first symbol denotes device technology, the second symbol denotes device function, and the third symbol denotes a wafer fab/assembly site code for internal tracking.

### EXAMPLES:

1. A PicoGate-Logic device with package code LR\* is an IDT74LVC1G79A.
2. A PicoGate-Logic device with package code GC\* is an IDT74ALVC1G04.

### PICOGATE-LOGIC (DY) PACKAGE SYMBOLIZATION GUIDELINES

TECHNOLOGY	CODE	FUNCTION	CODE
ALVC	G	00	A
ALVCH	J	02	B
LVC	L	04	C
LVCH <sup>(1)</sup>		U04	D
		06 <sup>(1)</sup>	
		07 <sup>(1)</sup>	
		08	E
		14	F
		32	G
		79	R
		86	H
		125	M
		126	N
		132 <sup>(1)</sup>	

### NOTE:

1. Code to be determined.