Integrated Device Technology, Inc.

FAST CMOS 10-BIT BUFFERS

IDT54/74FCT827AT/BT/CT/DT
IDT54/74FCT828AT/BT/CT

T-52-07

FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 3.8ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

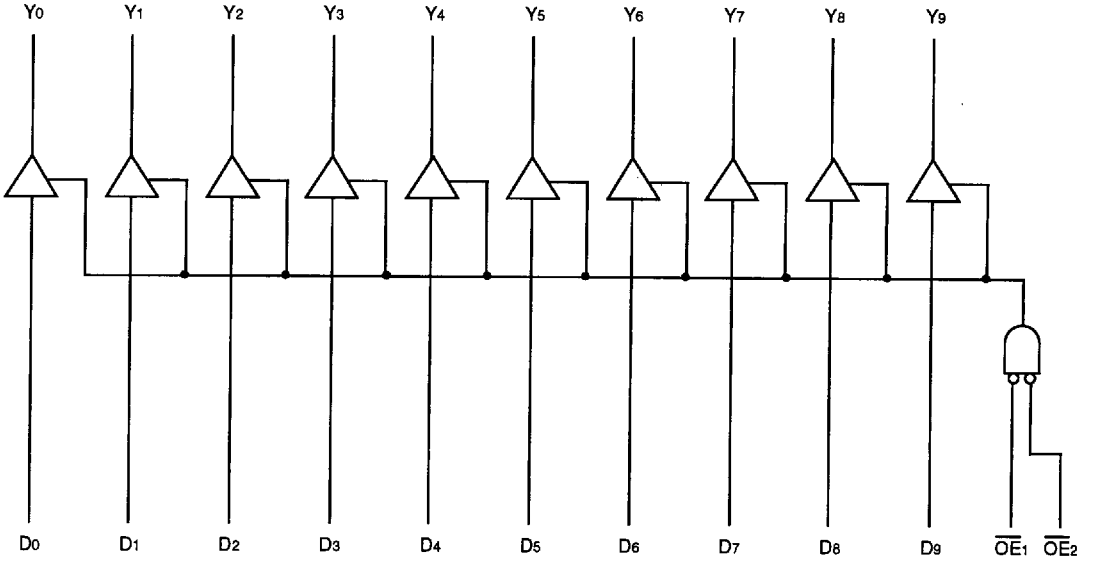
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827AT/BT/CT/DT and IDT54/74FCT828-AT/BT/CT 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



2573 drw 01

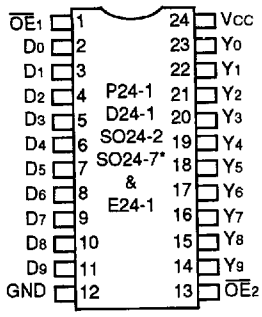
PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827AT/BT/CT/DT
Inverting	IDT54/74FCT828AT/BT/CT

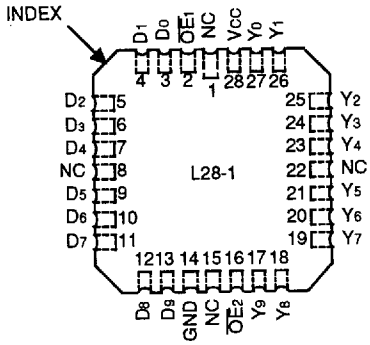
2573 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



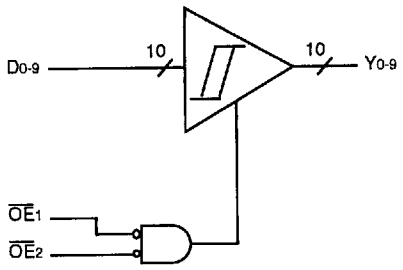
DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

* FCT827AT/BT/CT/DT only.

LOGIC SYMBOL



2573 cnv* 02-04

PIN DESCRIPTION

Names	I/O	Description
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2573 tbl 02

FUNCTION TABLES

IDT54/74FCT827T (NON-INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

2573 tbl 03

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

IDT54/74FCT828T (INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

2573 tbl 04

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2573 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2573 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2573 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND Eight Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2573 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	54/74FCT827AT/828AT				54/74FCT827BT/828BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
	IDT54/74FCT827T (Non-inverting)	CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	5.5	1.5	6.5	ns
	IDT54/74FCT828T (Inverting)	CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	16.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

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Symbol	Parameter	Conditions[1]	54/74FCT827CT/828CT				54/74FCT827DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.8	—	—	ns
	IDT54/74FCT827T (Non-inverting)	CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.5	—	—	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	—	—	—	—	ns
	IDT54/74FCT828T (Inverting)	CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	—	—	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.3	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.3	—	—	

2573 tbl 11

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.