# Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Package (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

#### description

The 'AC16472 and 'ACT16472 are noninverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (10EAB or 20EAB) and latch enable (1LEAB or 2LEAB) inputs. When 10EAB (or 20EAB) is low, the corresponding B outputs are active (high or low logic levels). When 10EAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when 1LEAB (or 2LEAB) is high and reflect the states of the corresponding A inputs when 1LEAB (or 2LEAB) is low.

## FUNCTION TABLE, EACH SECTION

INPUTS			D 01/78/170
LEAB	OEAB	LATCH DATA	B OUTPUTS
L	L	Current A Data	Current A Data
Н	L	Previous A Data	Previous A Data
L	Н	Current A Data	Z
Н	Н	Previous A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by OEBA and LEBA.

### 54AC16472, 54ACT16472 ... WD PACKAGE 74AC16472, 74ACT16472 ... DL PACKAGE (TOP VIEW)

10EAB	1	U 56	10EBA
1 LEAB	2	55	1 LEBA
1A1[	3	54	] 1B1
GND [	4	53	GND
1A2 [	5	52	] 1B2
1 A 3 🗌	6	51	] 1B3
V <sub>CC</sub> [	7	50	∏ V <sub>CC</sub>
1A4	8	49	184
1 <b>A</b> 5	9	48	□1B5
1A6	10	47	<b>□186</b>
GND [	11	46	GND
1A7 [	12	45	□1B7
1A8 [	13	44	☐1B8
1A9 [	14	43	□1B9
2 <b>A</b> 1	15	42	☐ 2B1
2A2	16	41	☐ 2B2
2A3 [	17	40	□ 2B3
GND [	18	39	E
2A4	19	38	2B4
2A5 🗌	20	37	285
2A6 L	21	36	2B6
Vcc [	22	35	∐ν <sub>cc</sub>
2A7	23	34	∐ 2B7
2A8 [	24	33	2B8
GND [	25	32	GND
2A9	26	31	H
2LEAB	27	30	
20EAB	28	29	20EBA

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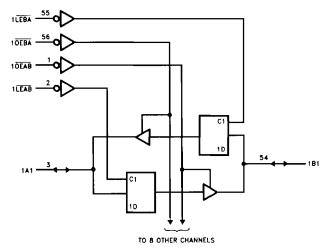
Data flow from B to A is similar, but uses 10EBA and/or 20EBA and 1LEBA and/or 2LEBA.

The 74AC16472 and 74ACT16472 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16472 has CMOS-compatible input thresholds. The 'ACT16472 has TTL-compatible input thresholds.

The 54AC16472 and 54ACT16472 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16472 and 74ACT16472 are characterized for operation from -40°C to 85°C.

## logic diagram (positive logic)



2LEBA C. 42 TO 8 OTHER CHANNELS

