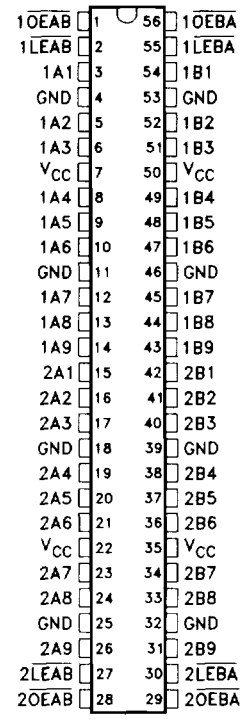
18-BIT LATCHED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0248—D3571, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16472, 54ACT16472 . . . WD PACKAGE
74AC16472, 74ACT16472 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16472 and 'ACT16472 are noninverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable ($1\overline{OEAB}$ or $2\overline{OEAB}$) and latch enable ($1\overline{LEAB}$ or $2\overline{LEAB}$) inputs. When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels). When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when $1\overline{LEAB}$ (or $2\overline{LEAB}$) is high and reflect the states of the corresponding A inputs when $1\overline{LEAB}$ (or $2\overline{LEAB}$) is low.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
$\overline{LEAB}$	$\overline{OEAB}$		
L	L	Current A Data	Current A Data
H	L	Previous A Data	Previous A Data
L	H	Current A Data	Z
H	H	Previous A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{OEBA}$ and $\overline{LEBA}$.

PRODUCT PREVIEW

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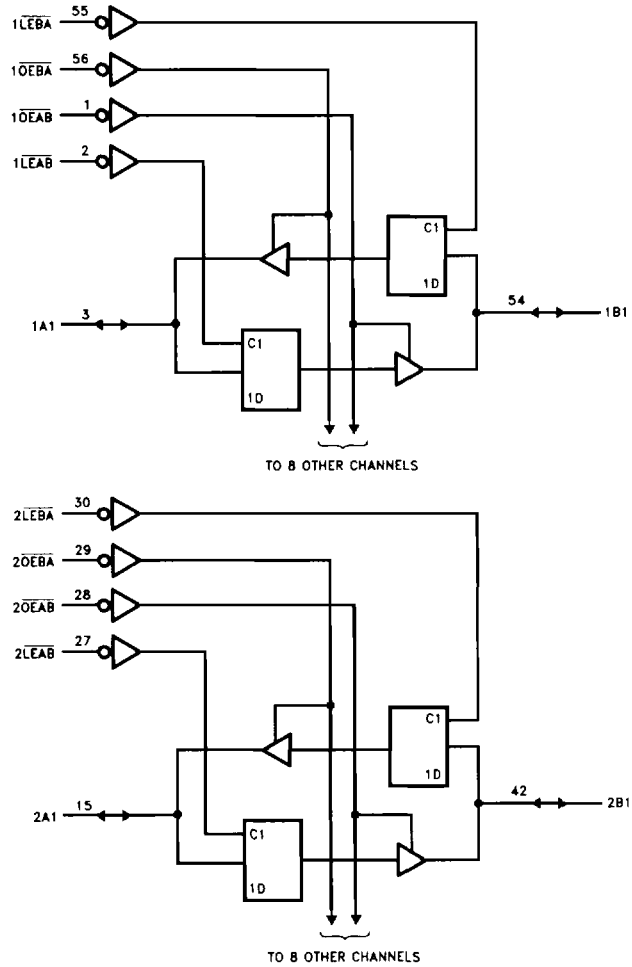
Data flow from B to A is similar, but uses $1\overline{OEBA}$ and/or $2\overline{OEBA}$ and $1\overline{LEBA}$ and/or $2\overline{LEBA}$.

The 74AC16472 and 74ACT16472 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16472 has CMOS-compatible input thresholds. The 'ACT16472 has TTL-compatible input thresholds.

The 54AC16472 and 54ACT16472 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16472 and 74ACT16472 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



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