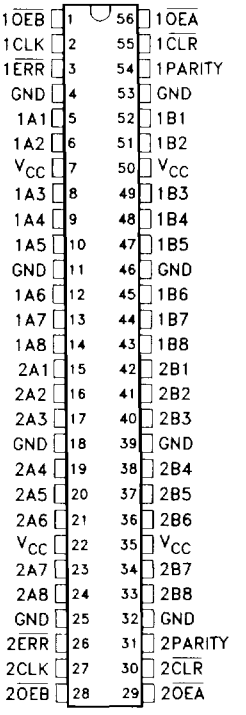
TI0271—D3547, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

**54AC16834, 54ACT16834 ... WD PACKAGE**
**74AC16834, 74ACT16834 ... DL PACKAGE**
**(TOP VIEW)**




## description

The 'AC16834 and 'ACT16834 contain two inverting 8-bit to 9-bit parity bus transceivers. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output ($1\overline{ERR}$ or $2\overline{ERR}$) is configured as an open-collector output. The B-to-A parity error flag is clocked into $1\overline{ERR}$ (or $2\overline{ERR}$) on the low-to-high transition of 1CLK (or 2CLK). $1\overline{ERR}$ (or $2\overline{ERR}$) is cleared (set high) by taking the clear input $1\overline{CLR}$ (or $2\overline{CLR}$) low.

The 74AC16834 and 74ACT16834 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

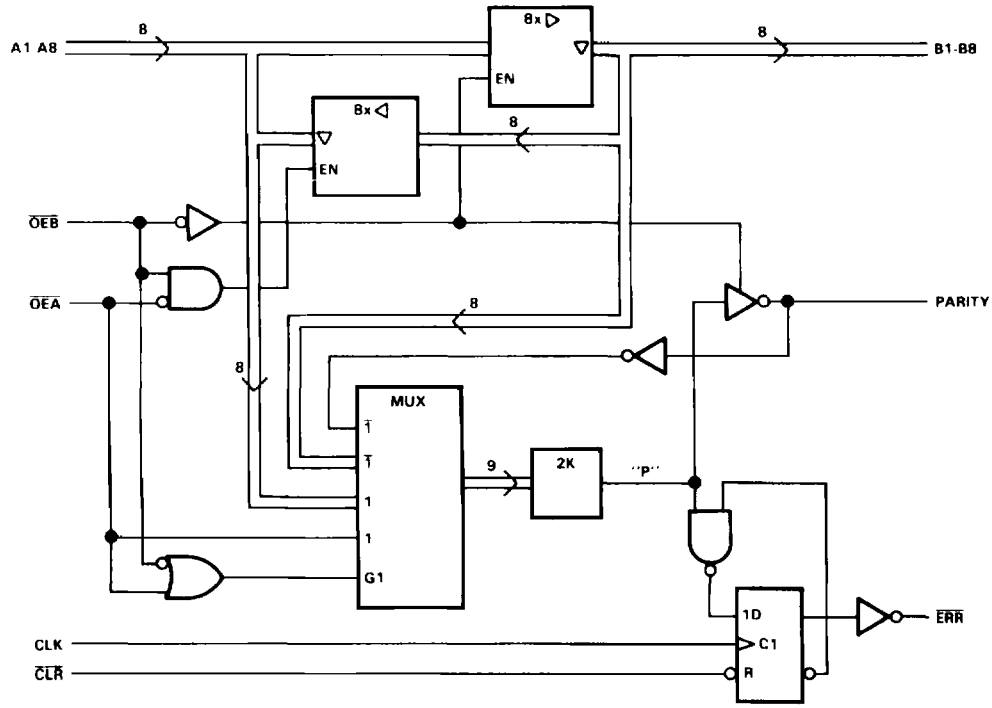
The 'AC16834 has CMOS-compatible input thresholds. The 'ACT16834 has TTL-compatible input thresholds.

The 54AC16834 and 54ACT16834 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16834 and 74ACT16834 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**logic diagram, each transceiver (positive logic)**




PRODUCT PREVIEW



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265