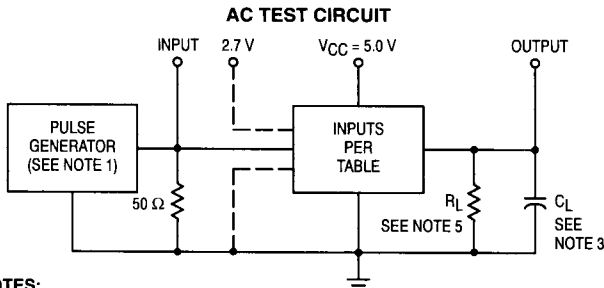
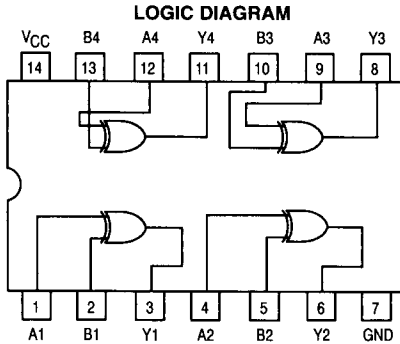




MOTOROLA

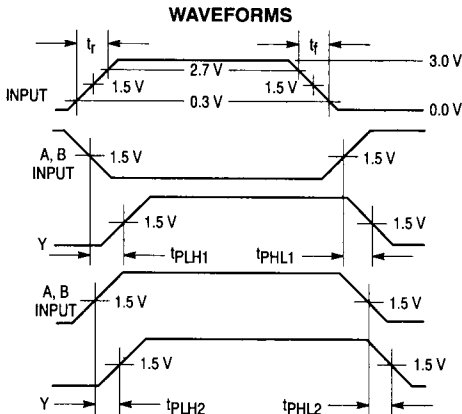
# Quad 2-Input Exclusive OR Gate

ELECTRICALLY TESTED PER:  
MIL-M-38510/34501



**NOTES:**

1. Input pulse generator has the following characteristics:  
 $t_r = t_f \leq 2.5$  ns, PRR  $\leq 1.0$  MHz.
2. Terminal condition, (pins not designated may be high  $\geq 2.0$  V, low  $\leq 0.8$ , or open).
3.  $C_L = 50$  pF  $\pm 10\%$ , including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5.  $R_L = 499 \Omega \pm 5.0\%$ .



## Military 54F86



**AVAILABLE AS:**

- 1) JAN: JM38510/34501BXA
- 2) SMD: N/A
- 3) 883: 54F86/BXAJC

**X = CASE OUTLINE AS FOLLOWS:**  
**PACKAGE: CERDIP: C**  
**CERFLAT: D**  
**LCC: 2**

**THE LETTER "M" APPEARS BEFORE THE / ON LCC.**

**PIN ASSIGNMENTS**

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	VCC
Y1	3	3	4	OPEN
A2	4	4	6	VCC
B2	5	5	8	VCC
Y2	6	6	9	OPEN
GND	7	7	10	GND
Y3	8	8	12	OPEN
A3	9	9	13	VCC
B3	10	10	14	VCC
Y4	11	11	16	OPEN
A4	12	12	18	VCC
B4	13	13	19	VCC
VCC	14	14	20	VCC

**BURN-IN CONDITIONS:**  
**VCC = 5.0 V MIN/6.0 V MAX**

**TRUTH TABLE**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



54F86

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA, V <sub>IL</sub> = 0.8 V, V <sub>IN</sub> = 2.0 V on other input.
V <sub>OL</sub>	Logical "0" Output Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IH</sub> = 2.0 V on both inputs.
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other input is open.
I <sub>IH1</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V, other input is open.
I <sub>IH2</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 7.0 V, other input is open.
I <sub>IL</sub>	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V, other input is open.
I <sub>OD</sub>	Diode Current	60		60		60		mA	V <sub>CC</sub> = 4.5 V, V <sub>IN</sub> = 5.5 V (both inputs), V <sub>OUT</sub> = 2.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V, other input = 0 V, V <sub>OUT</sub> = 0 V.
I <sub>CCH</sub>	Power Supply Current		18		18		18	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V, other input = 0 V.
I <sub>CC1</sub>	Power Supply Current		23		23		23	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (both inputs).
I <sub>CC2</sub>			28		28		28		V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (both inputs).
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at) V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL2</sub>	Propagation Delay /Data-Output Output High-Low	1.5 1.5	6.5 5.5	1.0 1.0	8.0 7.0	1.0 1.0	8.0 7.0	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω.
t <sub>PLH1</sub> t <sub>PLH2</sub>	Propagation Delay /Data-Output Output Low-High	1.5 1.5	7.0 5.5	1.0 1.0	8.5 7.0	1.0 1.0	8.5 7.0	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω.