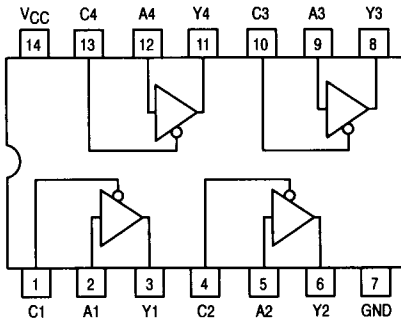




# Quad 3-State Buffer Low Enable

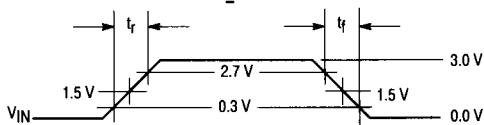
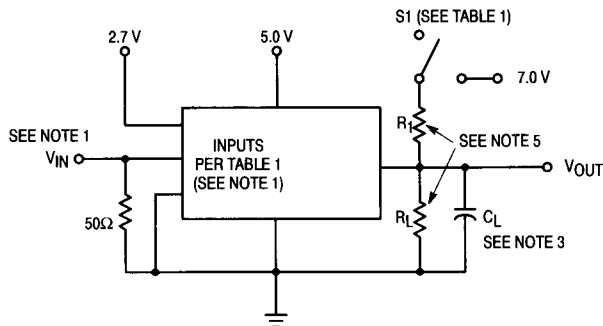
ELECTRICALLY TESTED PER:  
MPG54F125

LOGIC DIAGRAM



Positive Logic:  
Y = A  
Output is off (disabled) when C is high.

AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-39

## Military 54F125



AVAILABLE AS:

- 1) JAN: N/A
- 2) SMD: N/A
- 3) 883: 54F125/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
C1	1	1	2	GND
A1	2	2	3	VCC
Y1	3	3	4	OPEN
C2	4	4	6	GND
A2	5	5	8	VCC
Y2	6	6	9	OPEN
GND	7	7	10	GND
Y3	8	8	12	OPEN
A3	9	9	13	VCC
C3	10	10	14	GND
Y4	11	11	16	OPEN
A4	12	12	18	VCC
C4	13	13	19	GND
VCC	14	14	20	VCC

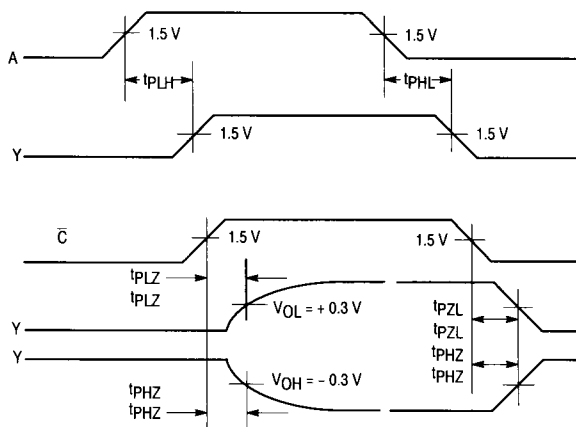
BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

FUNCTION TABLE

Inputs		Output
C	A	Y
L	L	L
L	H	H
H	X	(Z)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## WAVEFORMS



## NOTES:

1. Input pulse generator has the following characteristics: PRR = 1.0 MHz,  $t_r = t_f \leq 2.5$  ns and  $Z_{OUT} \approx 50 \Omega$ .
2. Terminal conditions (pins not designated may be high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).
3.  $C_L = 50$  pF  $\pm 10\%$  including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5.  $R_L = R_1 = 500 \Omega \pm 5.0\%$ .

Table 1

Test Type	S1
$t_{PLH}$	open
$t_{PHL}$	open
$t_{PHZ}$	open
$t_{PZH}$	open
$t_{PLZ}$	closed
$t_{PZL}$	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
$V_{OH}$	Logical "1" Output Voltage	2.4		2.4		2.4		V	$V_{CC} = 4.5$ V, $I_{OH} = -3.0$ mA, $V_{IN} = 2.0$ V, other input is = 0.8 V.
$V_{OL}$	Logical "0" Output Voltage		0.5		0.5		0.5	V	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA, $V_{IN} = 0.8$ V (both inputs).
$V_{IC}$	Input Clamping Voltage		-1.2					V	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA, other inputs are open.
$I_{IH}$	Logical "1" Input Current		20		20		20	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V, $V_{IN} = GND$ , other inputs are open.
$I_{IHH}$	Logical "1" Input Current		100		100		100	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IHH} = 7.0$ V, $V_{IN} = GND$ , other inputs are open.
$I_{IL}$	Logical "0" Input Current	0	-20	0	-20	0	-20	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IL} = 0.5$ V, other inputs are open.
$I_{IL}$	Logical "0" Input Current	0	-20	0	-20	0	-20	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IL} = 0.5$ V, other input = 0 V.
$I_{OS}$	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V, other input is GND, $V_{OUT} = GND$ .
$I_{IOZH}$	Output Off Current High		50		50		50	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IN} = 2.0$ V, other input = 0 V, $V_{OUT} = 2.7$ V.
$I_{IOZL}$	Output Off Current Low		-50		-50		-50	$\mu$ A	$V_{CC} = 5.5$ V, $V_{IN} = 2.0$ V, other input = 4.5 V, $V_{OUT} = 0.5$ V.
$I_{CCH}$	Power Supply Current		24		24		24	mA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V, other input = 0 V.
$I_{CCL}$	Power Supply Current		40		40		40	mA	$V_{CC} = 5.5$ V, $V_{IN} = 0$ V (all inputs).
$I_{CCZ}$	Power Supply Current Off		35		35		35	mA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V, other inputs are open.
$V_{IH}$	Logical "1" Input Voltage	2.0		2.0		2.0		V	$V_{CC} = 4.5$ V.
$V_{IL}$	Logical "0" Input Voltage		0.8		0.8		0.8	V	$V_{CC} = 4.5$ V.

## 54F125

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	- 55°C		
	Functional Tests	Subgroup 7		Subgroup 8A	Subgroup 8B	per Truth Table with $V_{CC} = 4.5\text{ V}$ , (Repeat at) $V_{CC} = 5.5\text{ V}$ , $V_{IL} = 0.5\text{ V}$ , and $V_{IH} = 2.4\text{ V}$ .

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Switching Parameters:	Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub>	Propagation Delay /Data-Output Output High-Low	3.0	7.5	3.0	9.0	3.0	9.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$
t <sub>PLH</sub>	Propagation Delay /Data-Output Output Low-High	2.0	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$
t <sub>PLZ</sub>	Propagation Delay /Data-Output Output Low-High	1.5	5.5	1.5	7.0	1.5	7.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$
t <sub>PHZ</sub>	Propagation Delay /Data-Output Output High-Low	1.5	5.0	1.5	7.0	1.5	7.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$
t <sub>PZL</sub>	Propagation Delay /Data-Output Output Low-High	3.0	8.0	3.0	10	3.0	10	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$
t <sub>PZH</sub>	Propagation Delay /Data-Output Output High-Low	3.0	7.5	3.0	9.0	3.0	9.0	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = R_1 = 500\ \Omega$

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