

# SN54F112, SN74F112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2932, MARCH 1987—REVISED JANUARY 1989

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

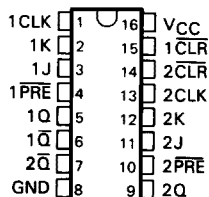
The SN54F112 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F112 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

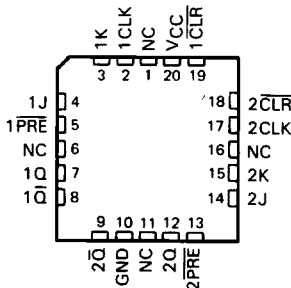
PRE		INPUTS			OUTPUTS	
		CLR	CLK	J	K	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$H^{\dagger}$	$H^{\dagger}$
H	H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	TOGGLE	
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

<sup>†</sup>The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F112 . . . J PACKAGE  
SN74F112 . . . D OR N PACKAGE  
(TOP VIEW)

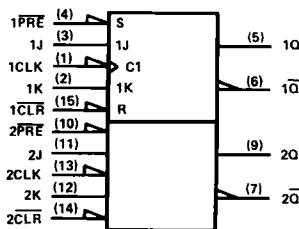


SN54F112 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

## logic symbol<sup>†</sup>

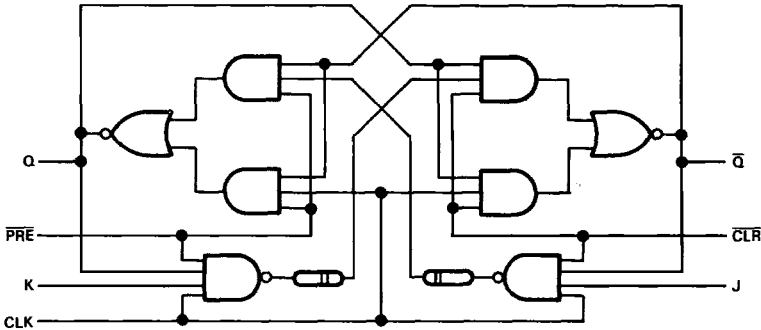


<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

2  
Data Sheets

**SN54F112, SN74F112**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage <sup>†</sup> .....	-1.2 V to 7 V
Input current .....	-30 mA to 5 mA
Voltage applied to any output in the high state .....	-0.5 V to $V_{CC}$
Current into any output in the low state .....	40 mA
Operating free-air temperature range: SN54F112 .....	-55°C to 125°C
SN74F112 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

<sup>†</sup>The input voltage ratings may be exceeded provided the input current ratings are observed.

**recommended operating conditions**

		SN54F112			SN74F112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			-18			-18	mA
$I_{OH}$	High-level output current			-1			-1	mA
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

2

Data Sheets

# SN54F112, SN74F112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F112			SN74F112			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75 \text{ V}$ , $I_{OH} = -1 \text{ mA}$				2.7			
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 20 \text{ mA}$		0.30	0.5		0.30	0.5	V
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	J or K	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.5 \text{ V}$			-0.6		-0.6
	PRE or CLR					-3		-3
	CLK					-2.4		-2.4
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0$		-60	-150		-60	-150	mA
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , See Note 1		12	19		12	19	mA

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $T_A = \text{MIN to MAX}^\S$				UNIT
		'F112		SN54F112		SN74F112		
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	110			0	100	MHz
$t_{\text{su}}$	Setup time before CLK↓	Data high	4			5		ns
		Data low	3			3.5		
$t_{\text{h}}$	Hold time after CLK↓	Data high	0			0		ns
		Data low	0			0		
$t_{\text{w}}$	Pulse duration	CLK high or low	4.5			5		ns
		CLR or PRE low	4.5			5		
$t_{\text{su}}$	Inactive-state setup time before CLK↓	PRE or CLR high	4			5		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = \text{MIN to MAX}^\S$				UNIT
			'F112			SN54F112		SN74F112		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			110	130			100			MHz
$t_{\text{PLH}}$	CLK	Q or $\bar{Q}$	1.2	4.6	6.5			1.2	7.5	ns
$t_{\text{PHL}}$			1.2	4.6	6.5			1.2	7.5	
$t_{\text{PLH}}$	PRE or CLR	Q or $\bar{Q}$	1.2	4.1	6.5			1.2	7.5	ns
$t_{\text{PHL}}$			1.2	4.1	6.5			1.2	7.5	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

¶ Inactive-state setup time is also referred to as "recovery time".

NOTES: 1.  $I_{CC}$  is measured with all outputs open, the Q and  $\bar{Q}$  outputs alternately high and the clock input grounded at the time of measurement.

2. Load circuits and waveforms are shown in Section 1.

2

Data Sheets

# 2

## Data Sheets