HARRIS

HI-508/883
HI-509/883

Single 8/Differential 4 Channel CMOS Analog Multiplexer

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low On Resistance (Max.) 400Ω**
- **Wide Analog Signal Range ..... ±15V**
- **TTL/CMOS Compatible ..... 2.4V (Logic "1")**
- **Access Time (Max.) 1000ns**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Replaces DG508A/DG508AA and DG509A/DG509AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

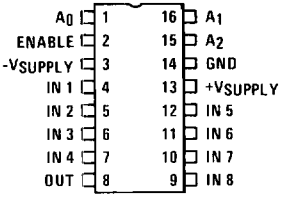
Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

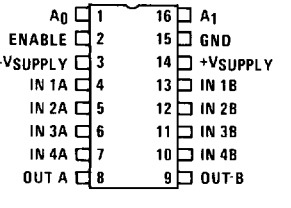
The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS. Switches are guaranteed to break-before-make, so that two channels are never shorted together. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and Maximum 0.8V for logic "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply. The HI-508/883 is an eight channel single-ended multiplexer, and the HI-509/883 is a four channel differential version. If input overvoltage protection is needed, the HI-548/883 and HI-549/883 multiplexers are recommended. For further information, see Application Notes 520 and 521.

Pinouts

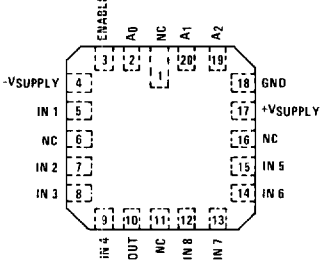
HI1-508/883 (CERAMIC DIP)
TOP VIEW



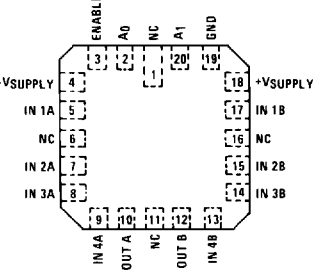
HI1-509/883 (CERAMIC DIP)
TOP VIEW



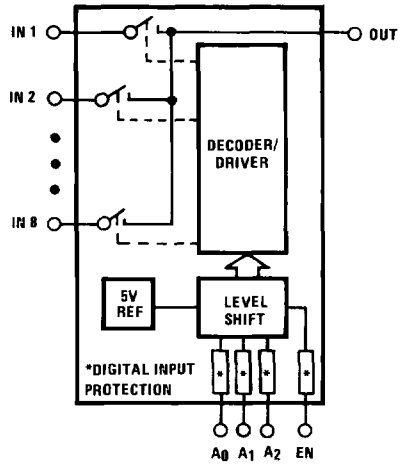
HI4-508/883 (CERAMIC LCC)
TOP VIEW



HI4-509/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

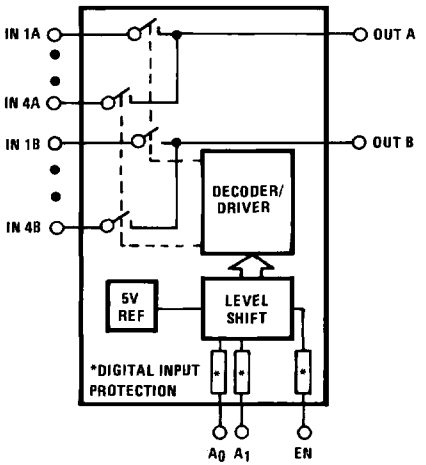


HI-508/883

TRUTH TABLES

HI-508/883

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8



HI-509/883

HI-509/883

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 22V
Analog Input Voltage
  $+V_S$ ..... $+V_{SUPPLY}$ +2V
  $-V_S$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage
  $+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
  $-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
  or 20mA, whichever occurs first.
Continuous Current, S or D 20mA
Peak Current, S or D
  (Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... 275°C
Junction Temperature ..... +175°C
Thermal Resistance, Junction-to-Case (θjc)
  Ceramic DIP Package ..... 21°C/W
  Ceramic LCC Package ..... 20°C/W
Thermal Resistance, Junction-to-Ambient (θja)
  Ceramic DIP Package ..... 83°C/W
  Ceramic LCC Package ..... 81°C/W
Power Dissipation (at 75°C)
  Ceramic DIP Package 1.20W
  Ceramic LCC Package 1.23W
Power Dissipation Derating Factor (Above +75°C)
  Ceramic DIP Package ..... 12.0mW/°C
  Ceramic LCC Package ..... 12.3mW/°C
ESD Classification ..... ≤2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) ..... 0V to 0.8V
Logic High Level (V_{AH}) ..... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1.0	1.0	µA
	I_{IL}		1, 2, 3	+25°C, +125°C -55°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(ON)}$	V_S = V_D = -10V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883		+125°C, -55°C	-100	+100	nA
Positive Supply Current	$I(+)$	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C		2.4	mA
Negative Supply Current	$I(-)$	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.4	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		300	Ω
		I_D = 1mA	2, 3	+125°C, -55°C		400	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		300	Ω
		I_D = -1mA	2, 3	+125°C, -55°C		400	Ω
Logic Level Voltage	V_{AL}	Note1	1, 2, 3	+25°C, +125°C,		0.8	V
	V_{AH}	Note 1	1, 2, 3	-55°C	2.4		V

NOTE 1. Used for forcing conditions for all DC tests unless otherwise specified.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 200Ω, C_L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V, f = 1MHz	2	+25°C		10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V HI-508/883	2	+25°C		45	pF
		f = 1MHz HI-509/883	2	+25°C		25	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	2	+25°C		12	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V	2	+25°C		10	mV
Off Channel Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	2, 3	+25°C	-50		dB

NOTE 2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

3. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

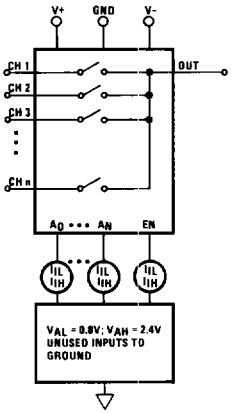
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

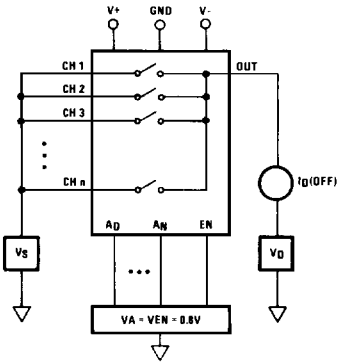
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

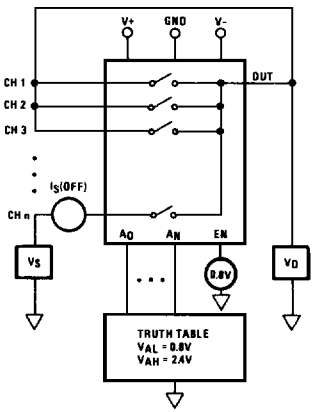
INPUT LEAKAGE CURRENT



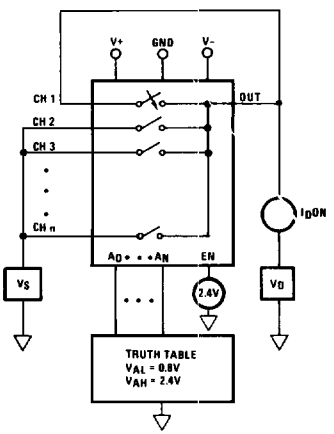
$I_{D(OFF)}$



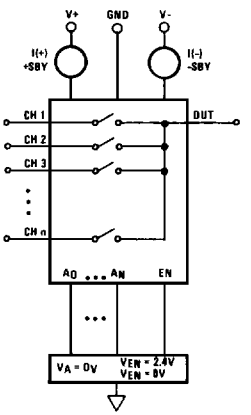
$I_{S(OFF)}$



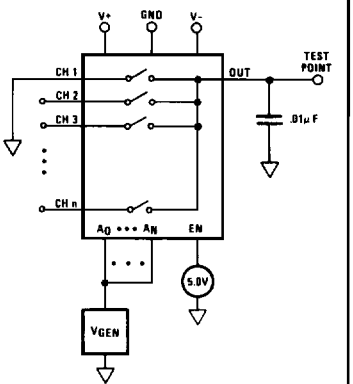
$I_{D(ON)}$



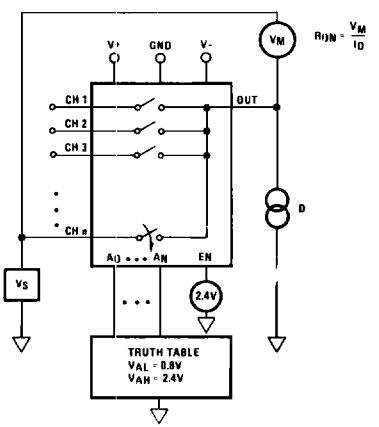
SUPPLY CURRENTS



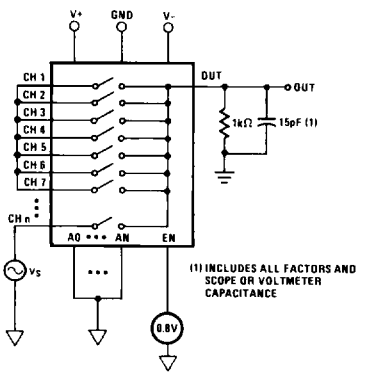
CHARGE TRANSFER ERROR



R_{DS}

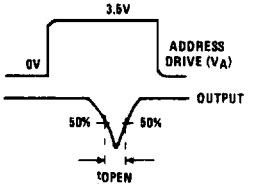


OFF CHANNEL ISOLATION

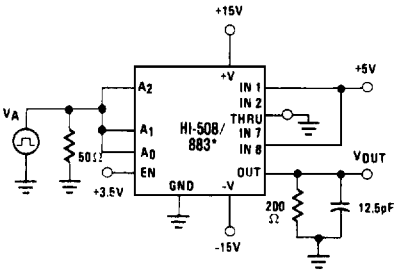


Switching Waveforms

ADDRESS DRIVE

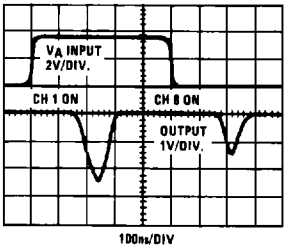


BREAK-BEFORE-MAKE DELAY (t_{OPEN})



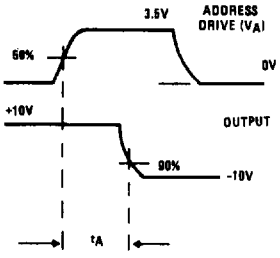
*SIMILAR CONNECTION FOR HI-509/883

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

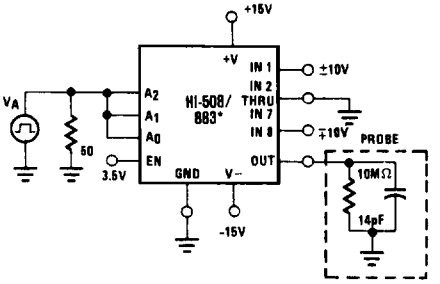


100ns/DIV

ACCESS TIME

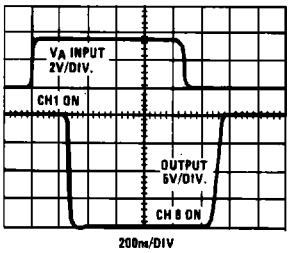


ACCESS TIME



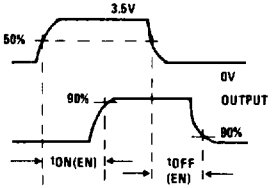
*SIMILAR CONNECTION FOR HI-509/883

ACCESS TIME

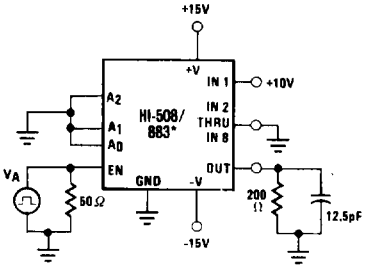


200ns/DIV

ENABLE DRIVE

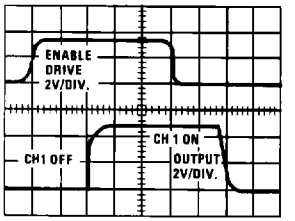


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



*SIMILAR CONNECTION FOR HI-509/883

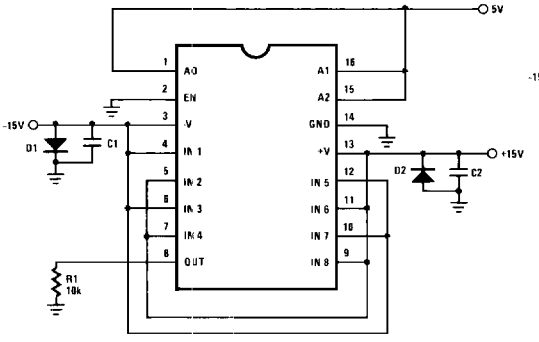
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



100ns/DIV

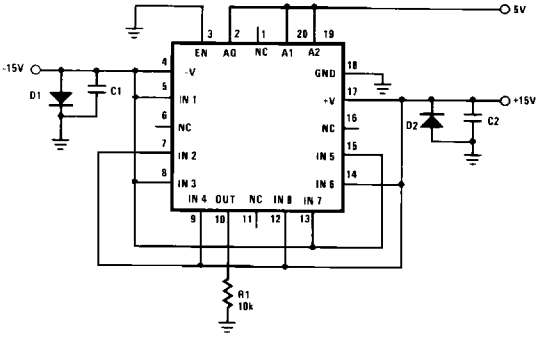
Burn-In Circuits

HI-508/883 CERAMIC DIP



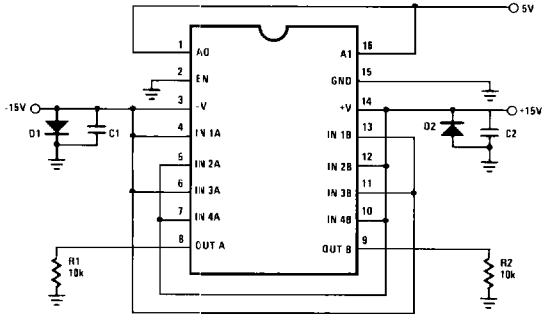
NOTES:
R1 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-508/883 LCC



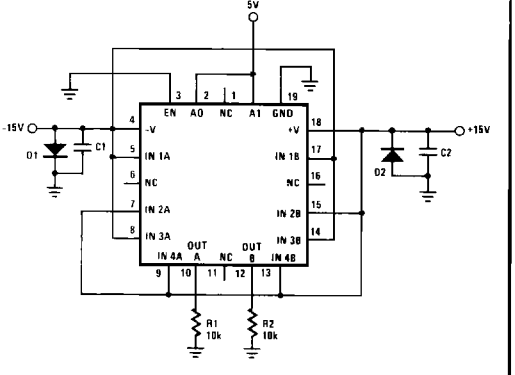
NOTES:
R1 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-509/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

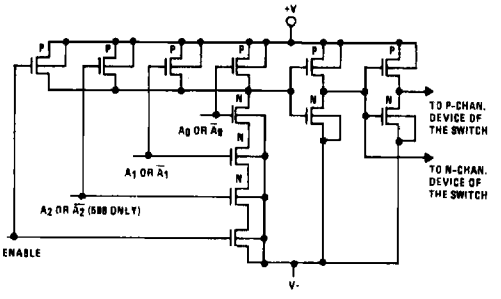
HI-509/883 LCC



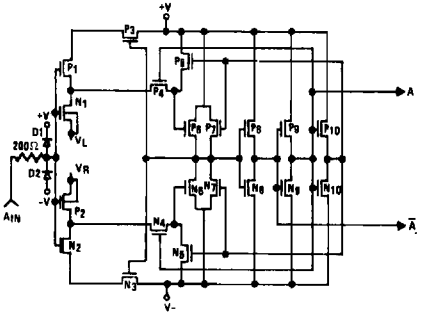
NOTES:
R1, R2 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS DECODER

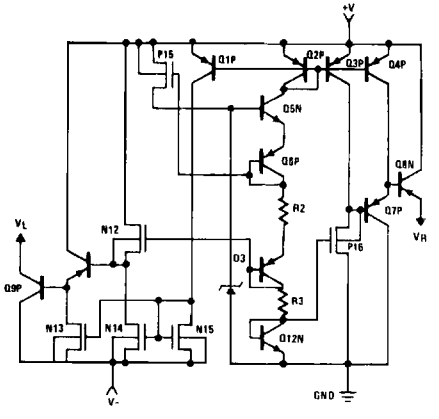


ADDRESS INPUT BUFFER LEVER SHIFTER

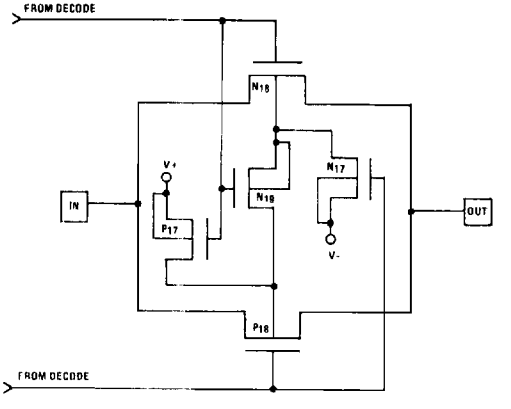


All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Die Characteristics

DIE DIMENSIONS: 81.9 x 90.2 x 19 mil

METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

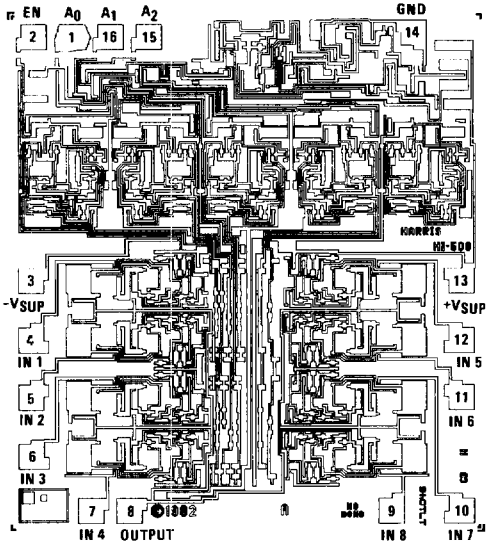
TRANSISTOR COUNT:
HI-508/883 243
HI-509/883 243

PROCESS: CMOS-DI

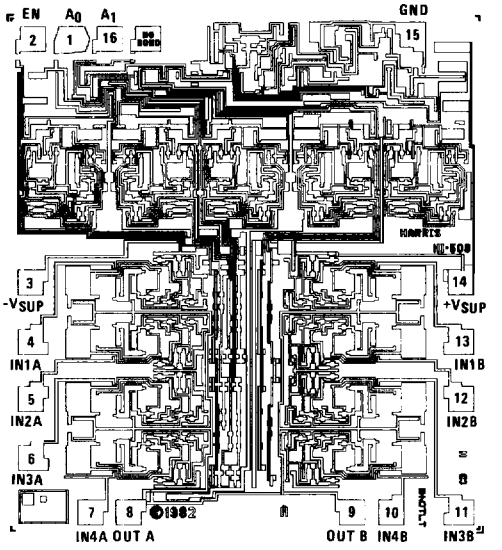
DIE ATTACH
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-508/883



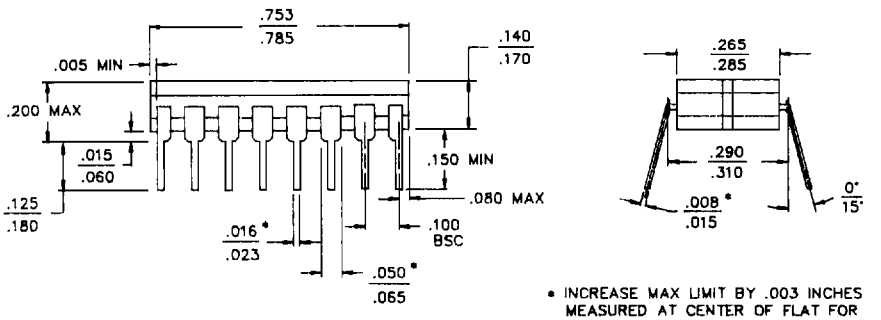
HI-509/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only.

Packaging†

16 PIN CERAMIC DIP

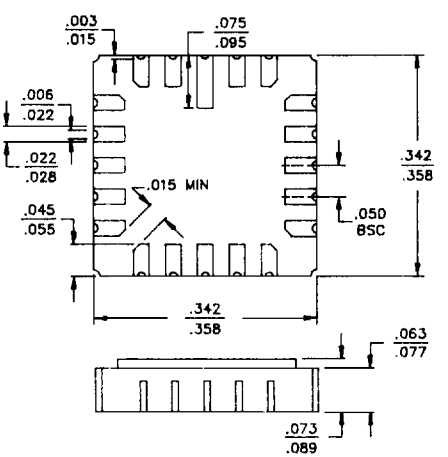


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

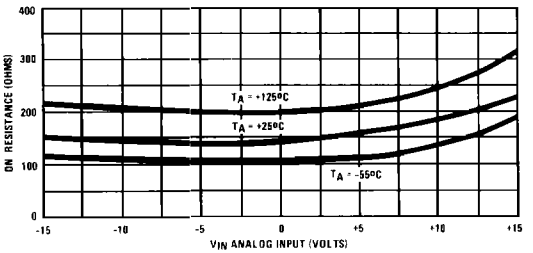
NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

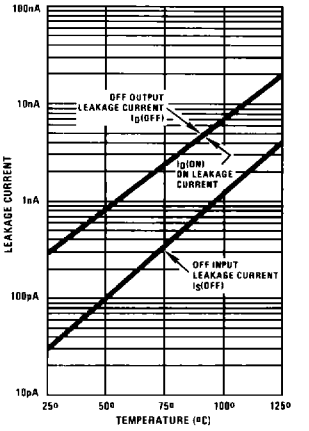
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +2.4V$, $V_{AL} = 0.8V$

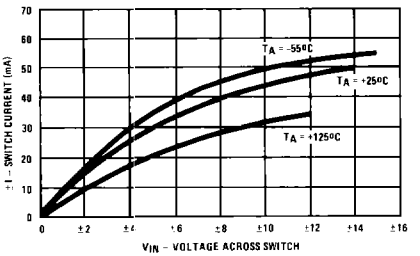
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



LEAKAGE CURRENT vs. TEMPERATURE



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY