HIGH-SPEED CMOS DUAL 4-INPUT MULTIPLEXER

IDT74FCT153AT/CT

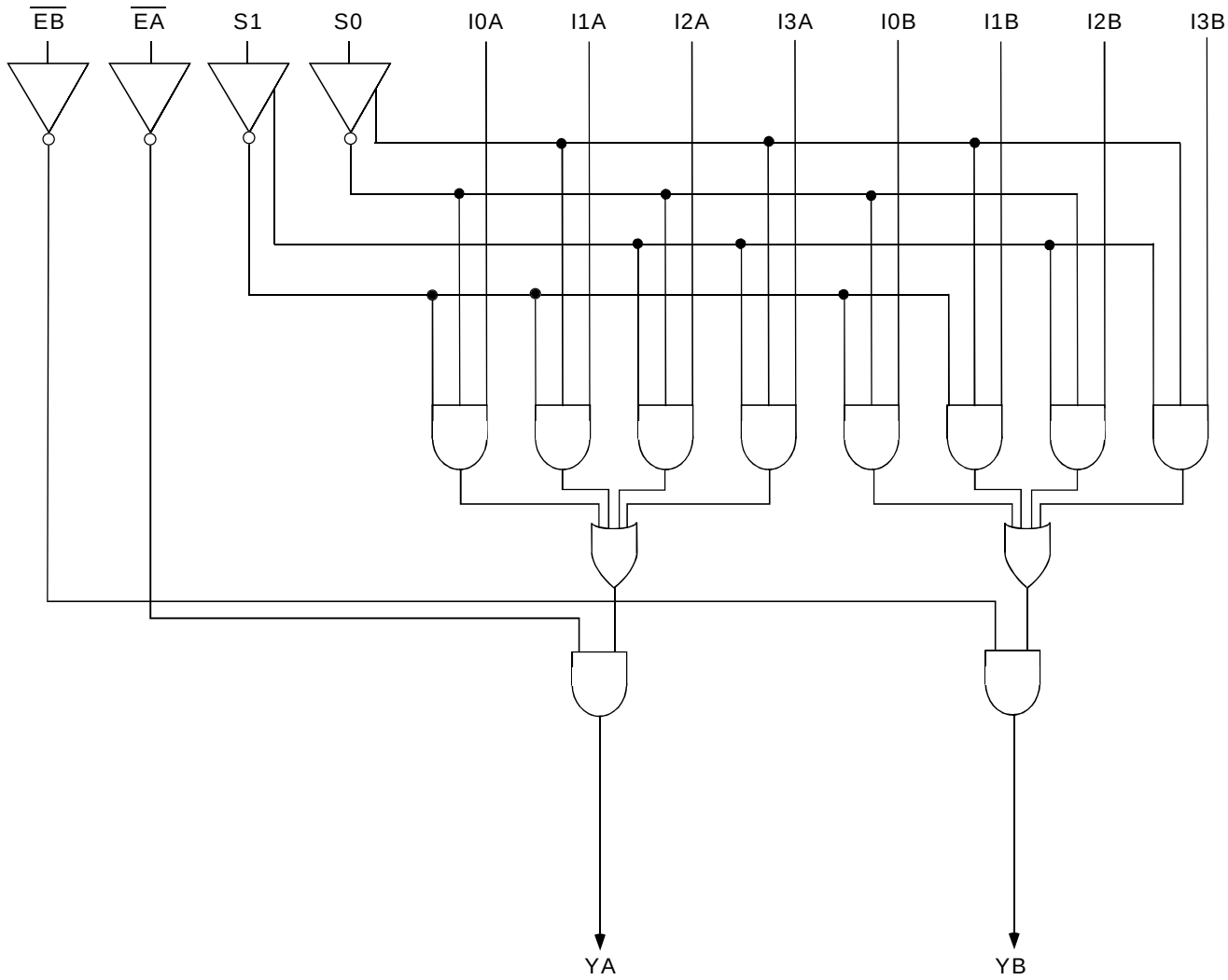
FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of –40°C to +85°C
- CMOS power levels: <7.5mW static
- Available in SOIC and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- JEDEC-FCT spec compatible
- A and C speed grades with 4.5ns t_{PD} for C
- I_{OL} = 48mA

DESCRIPTION:

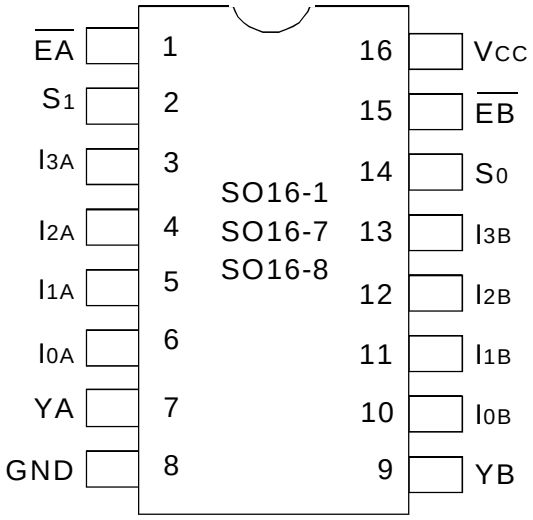
The IDT74FCT153T is a high-speed CMOS TTL-compatible dual 4-input multiplexer with TTL outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE **OCTOBER 1999**

PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	120	mA
I_{IK}	Continuous Clamp Current,	– 20	mA
I_{OK}	$V_I < 0$ or $V_O < 0$	– 50	mA

FCT Link

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
I_0 - I_7	I	Data In
S_0 - S_1	I	Select
$\overline{EA}$, $\overline{EB}$	I	Enable
YA, YB	0	Data Out

FUNCTION TABLE

Enable		Select				
$\overline{EA}$	$\overline{EB}$	S1	S0	YA	YB	Function
H	X	X	X	L	X	Disable A
X	H	X	X	X	L	Disable B
L	L	L	L	I_0A	I_0B	S_1- 0 = 0
L	L	L	H	I_1A	I_1B	S_1- 0 = 1
L	L	H	L	I_2A	I_2B	S_1- 0 = 2
L	L	H	H	I_3A	I_3B	S_1- 0 = 3

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	0 ≤ V_{IN} < Vcc	—	—	±5	µA
I_{IL}	Input LOW Current						
I_{OS}	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[2,3]		-60	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C[3]		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -15mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 48mA	—	—	0.5	V

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
3. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔI_{CC}	Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V freq = 0[2]	—	2	mA
I_{CCD}	Supply Current per Input per MHz	V_{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics..
2. Per TLL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

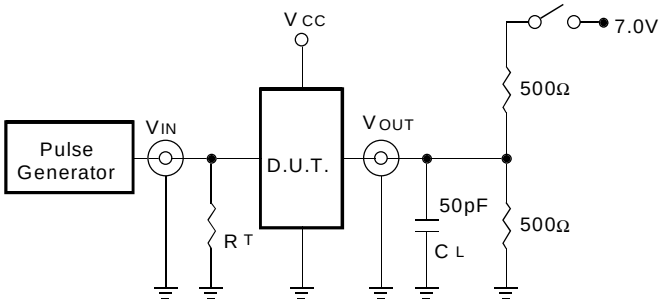
SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Symbol	Parameter[2]	74FCT153AT		74FCT153CT		Unit
		Min.	Max.	Min.	Max.	
t_{IY}	Propagation Delay Ixx to Yx	1.5	5.2	1.5	4.5	ns
t_{SY}	Propagation Delay Sx to Yx	1.5	6.6	1.5	5.6	ns
t_{OEH} t_{OEL}	Output Enable Time $\overline{Ex}$ to Yx	1.5	5.2	1.5	4.8	ns

NOTES:
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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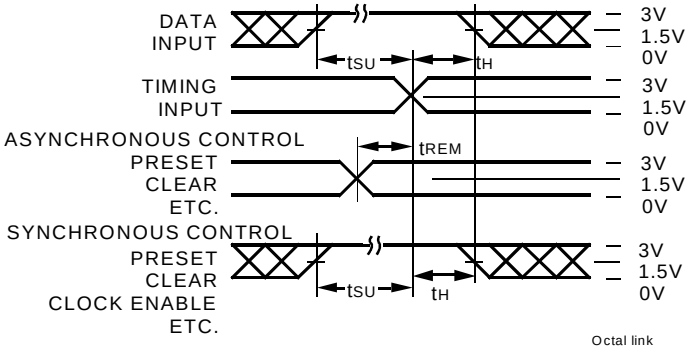
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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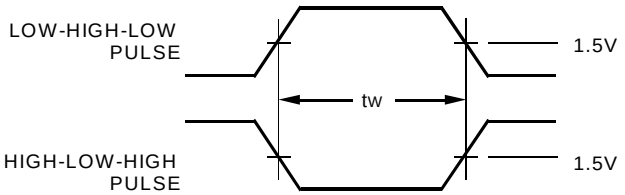
PULSE WIDTH



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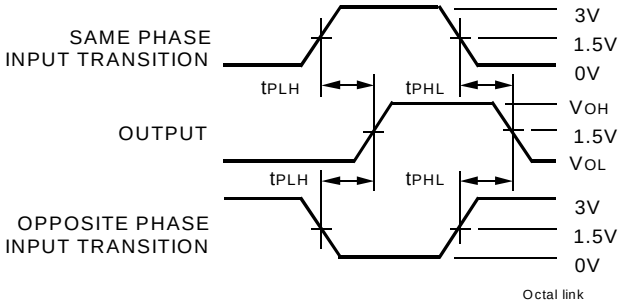
PROPAGATION DELAY



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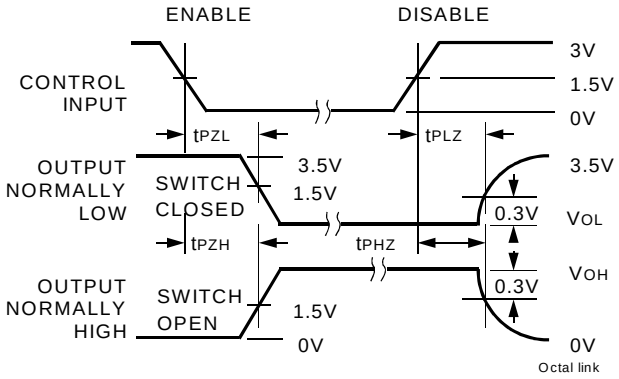
ENABLE AND DISABLE TIMES



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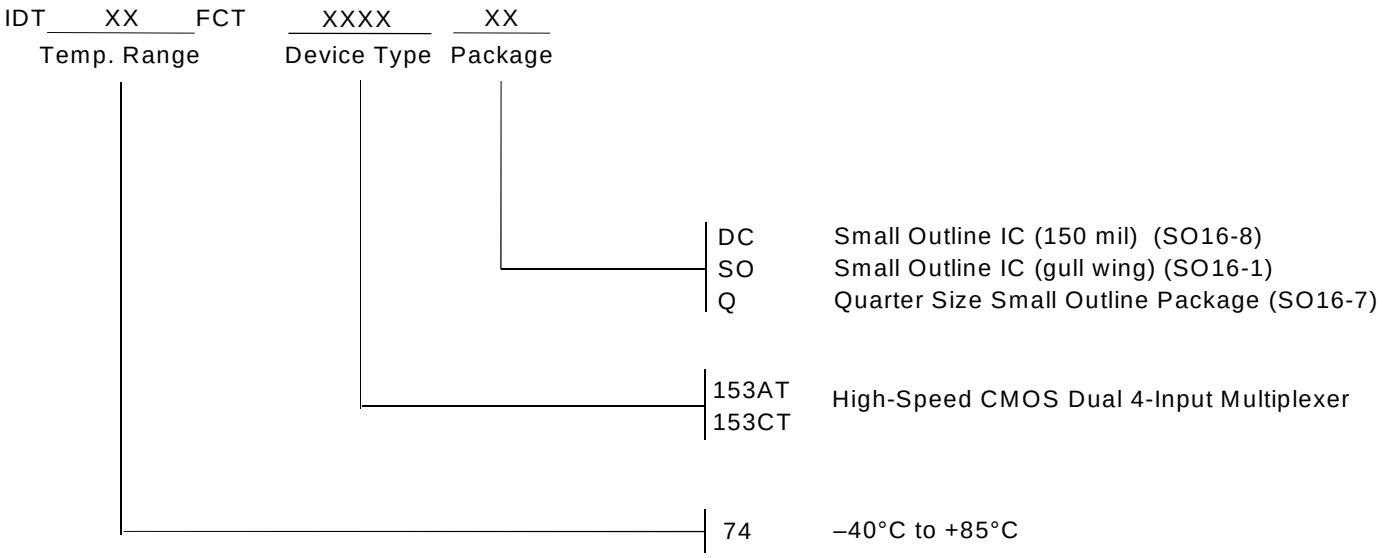
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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