1.0 Features

- Generates up to nine clock outputs, grouped as 4-4-1 from one reference clock input
- Pin enable/disable of two banks of four clocks
- Auto power-down shuts off PLL, brings outputs low in the absence of any REF input
- Tracking skew < 200ps (spread-spectrum tolerant)
- Input-to-output propagation delay < 200ps
- Available in a 16-pin 0.150" SOIC

Figure 1: Block Diagram

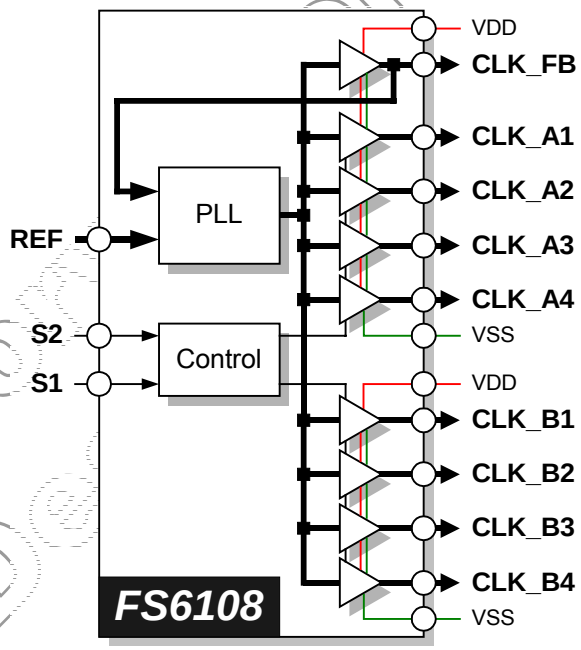

Table 1: Clock Enable Configuration

CONTROL		CLOCK OUTPUTS (MHz)			
S2	S1	CLK_A1:4	CLK_B1:4	CLK_FB	Source
0	0	Tristate	Tristate	Driven	PLL
0	1	Driven	Tristate	Driven	PLL
1	0	Driven	Driven	Driven	REF
1	1	Driven	Driven	Driven	PLL

Figure 2: Pin Configuration

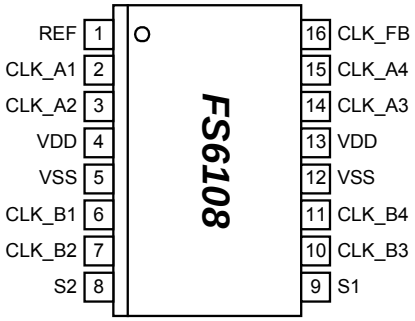

Table 2: Pin Descriptions

Key: DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION	
2	DO_D	CLK_A1	Clock output	Bank A
3	DO_D	CLK_A2	Clock output	
14	DO_D	CLK_A3	Clock output	
15	DO_D	CLK_A4	Clock output	
6	DO_D	CLK_B1	Clock output	Bank B
7	DO_D	CLK_B2	Clock output	
10	DO_D	CLK_B3	Clock output	
11	DO_D	CLK_B4	Clock output	
16	DO_D	CLK_FB	Clock output that also provides an internal feedback connection to the PLL	
1	DI_D	REF	Reference clock input	
8, 9	DI^U	S2, S1	Two select inputs that enable and disable the clock outputs, and enable or bypass the PLL	
4, 13	P	VDD	3.3V power supply	
5, 12	P	VSS	Ground	

2.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Operating Temperature Range	T_A		0		70	°C
Load Capacitance	C_L	CLK_A1:4, CLK_B1:4, CLK_FB			30	pF
Reference Frequency Range	f_{REF}		10		66.67	MHz

Table 5: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.6V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{REF} = 66.6MHz; all supplies = 3.465V		36		mA
Supply Current, Static	I_{DDs}	REF stopped either high or low		20		µA
Reference Input (REF)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current (pull-down)	I_{IH}	V_{IH} = 3.3V		25		µA
Low-Level Input Current	I_{IL}		-1		1	µA
Digital Inputs (S1, S2)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}		-1		1	µA
Low-Level Input Current (pull-up)	I_{IL}	V_{IL} = 0V		-30		µA
Clock Outputs (CLK_A1:4, CLK_B1:4, CLK_FB)						
High Level Output Source Current	I_{OH}	V_O = 2.4V	-7	-65		mA
Low Level Output Sink Current	I_{OL}	V_O = 0.4V		26	7	mA
Output Impedance	z_{OL}	Measured at 1.5V, output driving low		20		Ω
	z_{OH}	Measured at 1.5V, output driving high		18		
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_{DD} = 3.6V, V_O = 0V; shorted for 30s, max.		-96		mA
Short Circuit Output Sink Current	I_{OSL}	V_{DD} = V_O = 3.6V, shorted for 30s, max.		90		mA

Table 6: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.6V, no load on any output, and ambient temperature range T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Clock Outputs (CLK_A1:4, CLK_B1:4, CLK_FB)						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=30pF		75		ps
Skew, Tracking	$t_{sk(tr)}$	±0.5% non-linear (Lexmark) profile @ 31.5kHz		190		ps
Skew, Bank Output-Bank Output	$t_{sk(b)}$	CLK_A2 to CLK_B1; C_L=30pF		250		ps
PLL Reference Zero Delay	t_Φ	REF to CLK_FB		150		ps
Rise Time *	t_r	Measured @ 0.8V – 2.0V; C_L=30pF		1.6		ns
Fall Time *	t_f	Measured @ 2.0V – 0.8V; C_L=30pF		1.0		ns

3.0 Package Information

Table 7: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

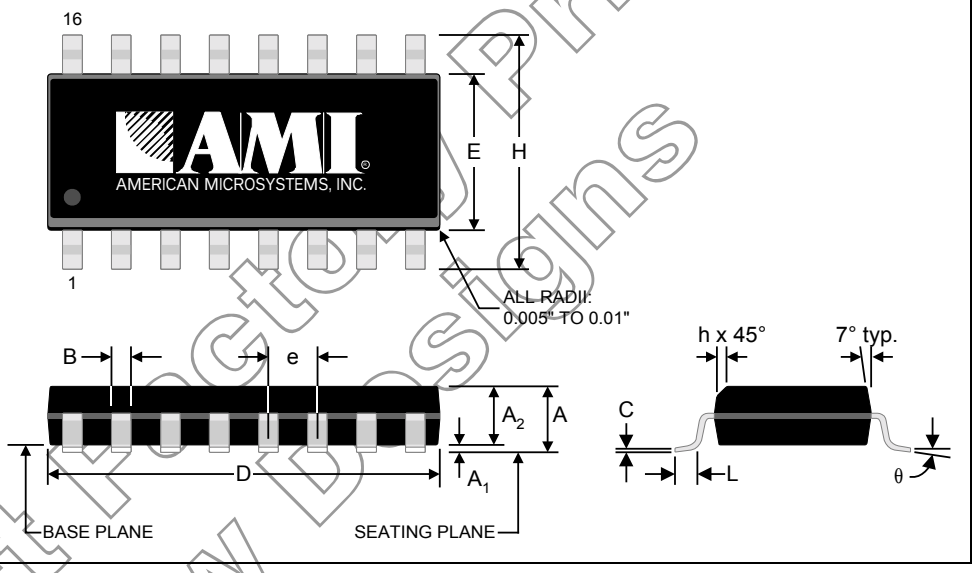

Table 8: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	109	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

4.0 Ordering Information

Table 9: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6108-01	12055-801	16-pin (0.150") SOIC	0°C to 70°C (Commercial)	Tape and Reel
	12055-801	16-pin (0.150") SOIC	0°C to 70°C (Commercial)	Tubes

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